1/10 inch VGA SOC CMOS Image Sensor With DVP and SPI

BF20A6

Datasheet

Apply to：BF20A6CS、BF20A6CS-T

Content

1. General Description

The BF20A6 is a 1/10-inch VGA CMOS Image Sensor which includes CMOS image sensor (CIS) and ISP. It is fabricated with the world's most advanced CIS process to realize ultra-low dark noise, high sensitivity, high dynamic range and very low power imaging system. The sensor consists of a 640×480 pixel array which has an optical format of 1/10 inch for VGA. It has integrated noise canceling CDS circuits, analog global gain and separated R/G/B gain controller, automatic black level compensation and on-chip 10-bit ADC. The on-chip ISP provides a very smooth AE and accurate AWB control. It provides various data formats, such as Bayer RGB, YCbCr 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

The product is capable of operating at up to 30 frames per second at 12MHz master clock in VGA mode, with complete user control over image quality and data format. All required image processing functions are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/10 inch for VGA
- 30 frames/sec VGA mode.
- Ultra-low dark noise at high temperature.
- Ultra-Low power consumption
- ≤70 mW@30fps VGA
- ≤180 uA @ power down
- Output formats: YUV422/Raw/ Only Y
- Power supply: 1.8/ 2.8V for I/O, 2.8V for VDD3A/VDD3D
- Horizontal /Vertical mirror.
- Auto black level control.
- Image processing function: Gamma Correction, Bad Pixel Correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, Skin Detection, and Data Format Conversion. Exposure control, Gain control, Test pattern, Image size control, Lens shading, Gamma and so on.
- Package: CSP.

3. Applications

- Cellular Phone Cameras
- Notebook PC cameras
- PDAs
- MP4
- Digital still cameras and camcorders
- Video telephony and conferencing equipment.

4. Technical Specifications

- Active pixel array: 640*480
- Pixel size: 2.25um×2.25um
- Sensitivity: 1.35V/Lux-sec
- Dark current: ≤2 mV/s at 25℃
- Power supply: 2.8V/1.8V
- Power consumption: ≤70 mW@30fps (VGA)
- Standby current: ≤180 uA
- S/N Ratio: 37 dB
- Dynamic range: 60 dB
- Operating temperature: -10~65℃
- Stable Image temperature: 0~60℃
- Optimal lens chief ray angle: 28° non-linear
- Package: CSP

5. Functional Overview

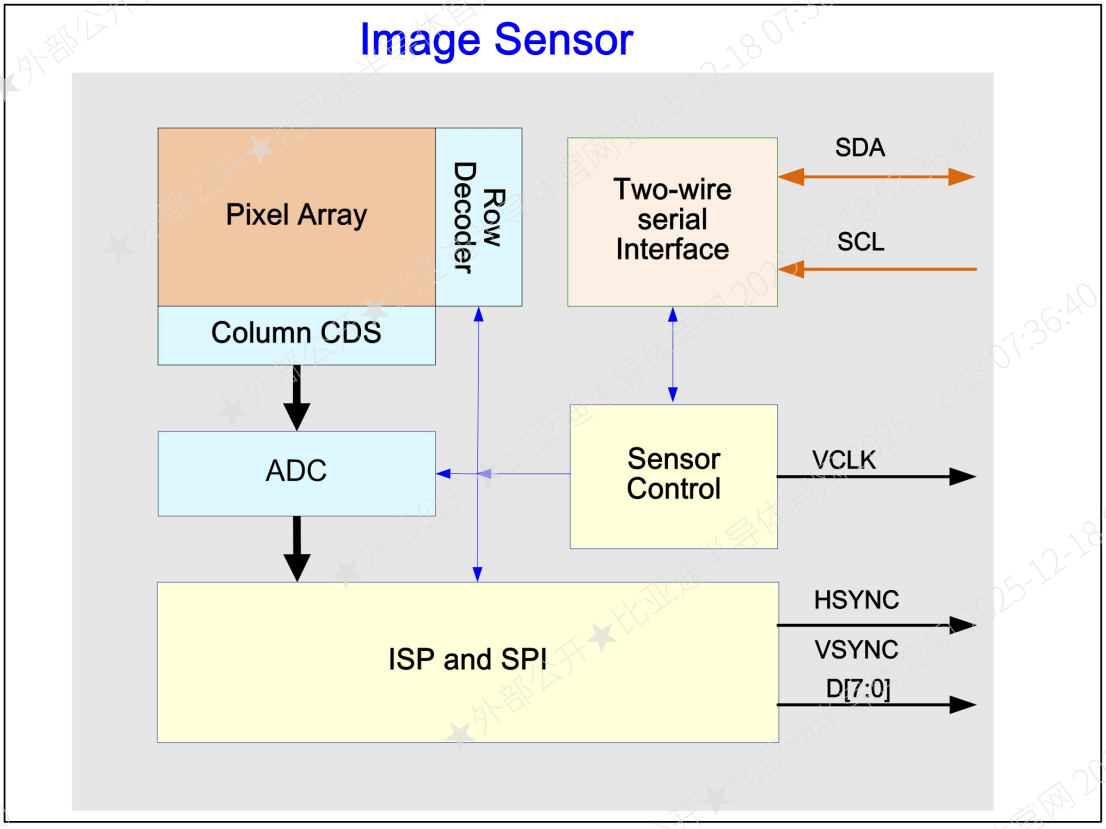


Figure 1. Block Diagram

BF20A6 has an active image array of 640x480 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The

analog signal is transferred to digital signal by A/D converter. It provide global gain to get accurate exposure under different light condition. The digital signals are controlled by Sensor control Block, including Exposure control, Gain control, Test pattern, Image size control and so on.

BF20A6 has on-chip PLL, it can be used by via two-wire serial interface bus setting.

5.1 Pixel Array

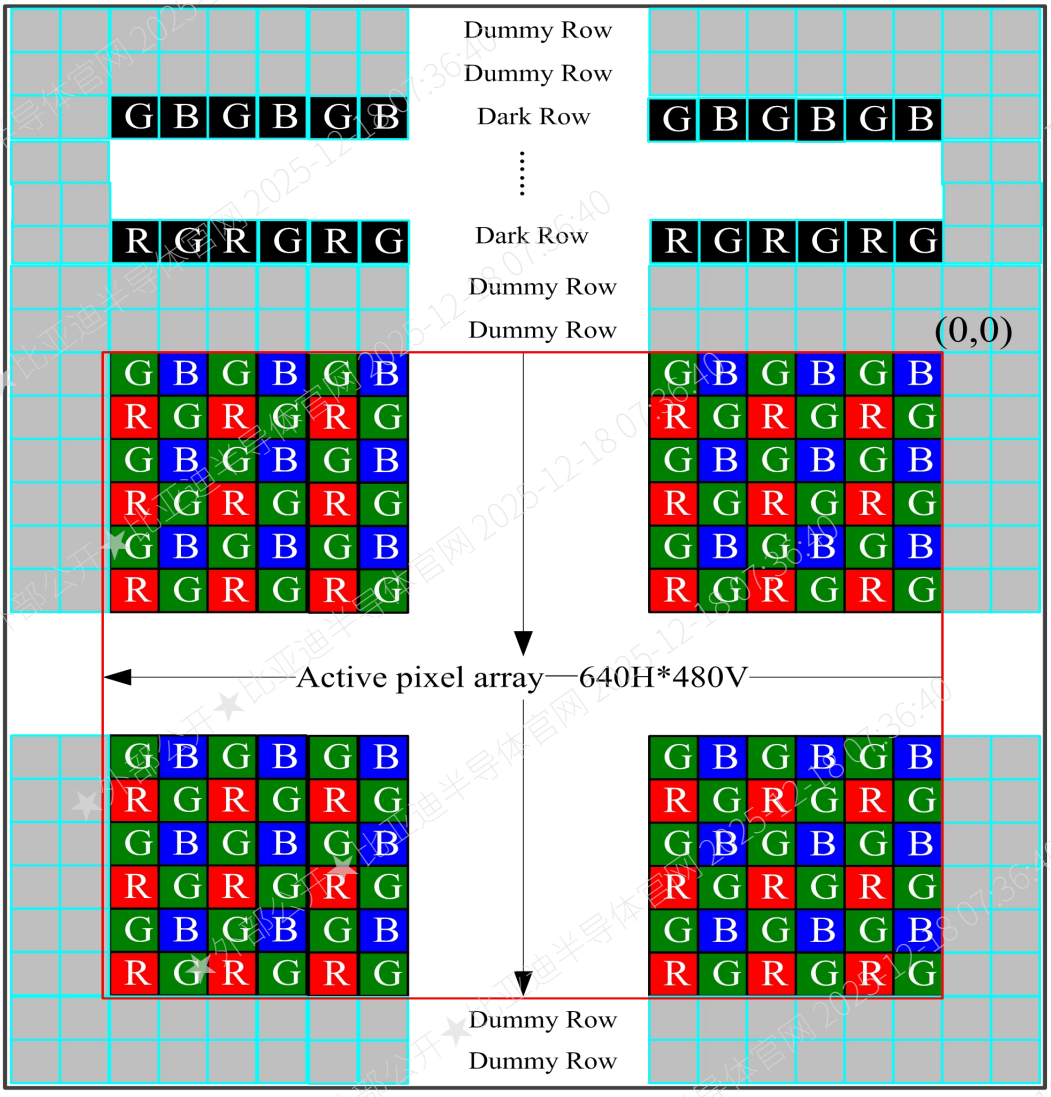


Figure 2. Sensor Array Region

The pixel array includes 640x480 effective pixels for imaging, whose address range is from (0, 0) to (639, 479). There are extra dark rows at the top side for black level control.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF20A6 can provide the Raw Bayer data , YUV data and Only Y through SPI and DVP interface. If flip or not in column.

5.2 Lens Chief Ray Angle (CRA)

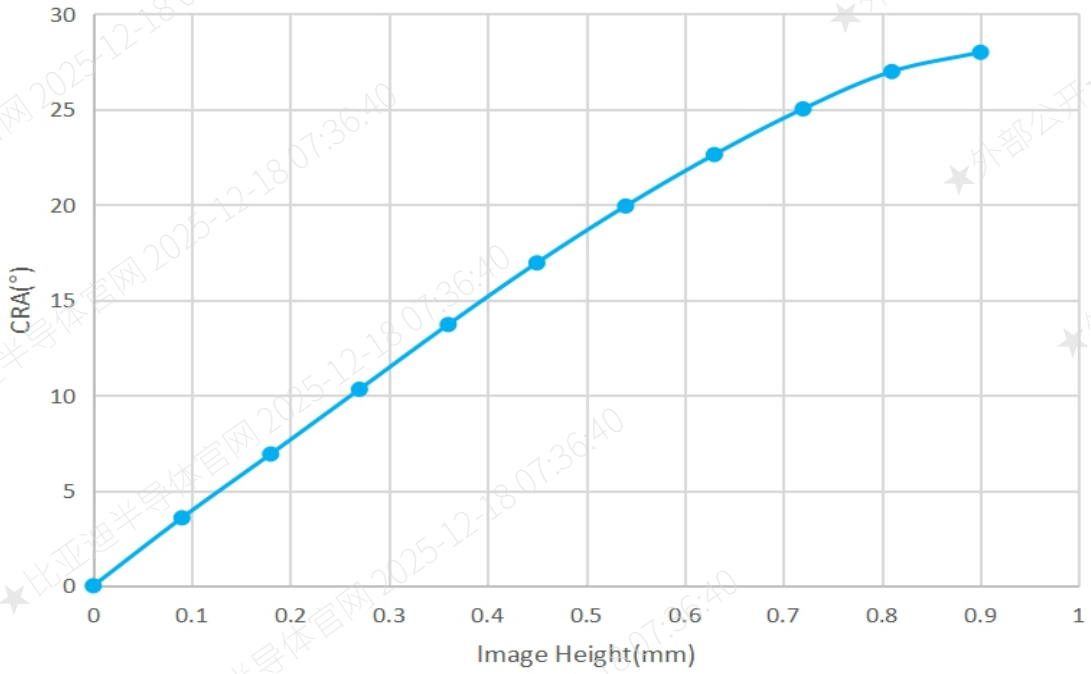


Figure 3. CRA information

Table 1. CRA versus image height plot

Field	Image Height(mm)	CRA(degree)
0	0	0
10%	0.09	3.57
20%	0.18	6.91
30%	0.27	10.31
40%	0.36	13.71
50%	0.45	16.95
60%	0.54	19.93
70%	0.63	22.63
80%	0.72	25.03
90%	0.81	26.99
100%	0.9	28.00

5.3 Column CDS

BF20A6 has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer and ADC circuit remove column level FPN caused by various sources of

manufacturing process variations.

5.4 Sensor control

- Array control and frame generation
- Internal timing signal generation and distribution
- Exposure control, Gain control, Test pattern,
- Image size control
- Frame rate timing

5.5 A/D converter

The analog signals are converted to digital forms and data are streamed out column by column. BF20A6 provides the 10-bit Raw Bayer data through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level control calculates the data of the dark row and controls the lowest black level for output image data.

6. Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.1 V
- Supply voltage (VDD3A/VDD3D): 2.7~ 3.1V
- Operating temperature: -10℃~65℃
- Storage temperature: -40℃~85℃
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2 DC Parameters

Table 2. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	1.8	3.1	1
VDD3A	Analog power supply	V	2.7	2.8	3.1	--
VDD3D	Analog power supply	V	2.7	2.8	3.1	--
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
I_vddio	VDDIO supply current, normal operation mode	mA	--	15	22	
I_vdd3d	VDD3D supply current,	mA	-- --	1	2	2
I_vdd3a	VDD3A supply current,	mA	--	9	15	2

Note:

1. VDDIO=1.8V/ 2.8V （30 fps）
2. The Current of power is decided by the work mode, ex. Frequency of clock and output format. The Max. Current will not appear at the same time.

6.1.3 Clock Requirement

Table 3. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External input clock	MHz	--	24	--	1
PCLK	Pixel clock of the system	MHz	--	12	--	2
VCLK	DVP Output clock	MHz	--	24	--	3
SCLK	two-wire serial interface clock frequency	KHz	--	400	--	4

Note:

1. XCLK is the input clock of system as the input of PLL.
2. PCLK is the pixel clock of system, and it is generated by PLL.
3. VCLK is the DVP output clock when the VCLK Pin is defined. (Raw：VCLK=PCLK；YUV：VCLK=2*PCLK)
4. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section

6.2 Electro-Optical Characteristics

Clock frequency: 12MHz.
Operating voltage: VDDIO=2.8V, VDD3D=2.8V, VDD3A=2.8V.
Operating temperature: 25°C

Table 4. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	1.35		1
Dark current	mV/sec	--	1	--	2
S/N ratio	dB	--	37	--	--
Dynamic Range	dB	--	60	--	--
Frame Rate	fps	--	30	30	3

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (25 Celsius).
3. With 640×480 at PCLK 12MHz.

6.3 Timing

6.3.1 The inner VGA Fame Timing

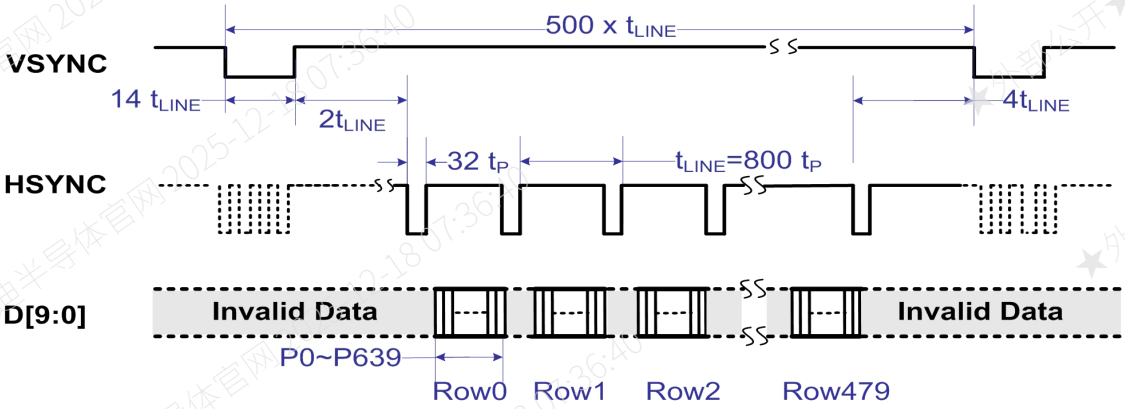


Figure 4. Inner VGA Frame Timing

Table 5. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	Pixel clock period	--	83.3	--	ns
f_{PCLK}	Pixel Clock Frequency	--	12	--	MHz
t_{LINE}	Line length	--	800x t_P	--	ns

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

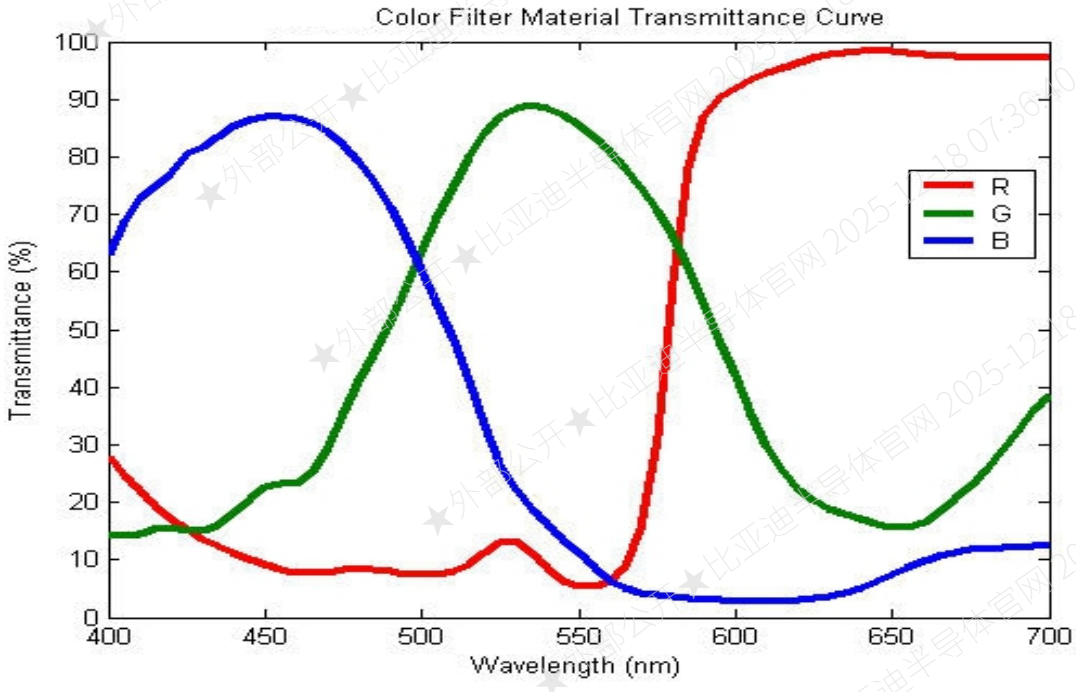


Figure 5. Spectral Characteristics

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF20A6 are written and read through the two-wire serial interface. BF20A6 has two-wire serial interface slave. BF20A6 is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF20A6 through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF20A6 is 7'b1101110 (0X6e), it doesn't include W/R bit.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF20A6 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

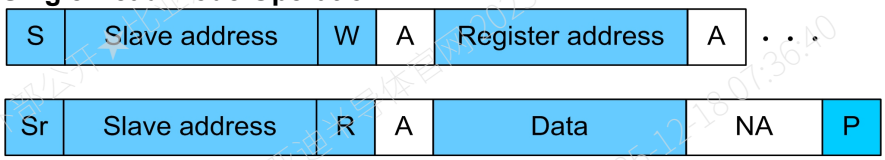
A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

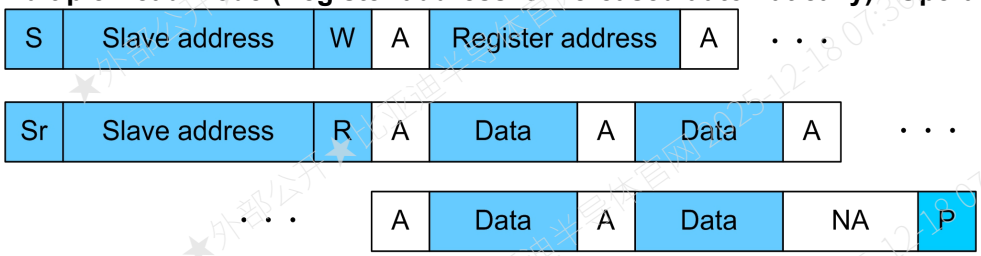
Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] operation

Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) [1] Operation



From master to slave From slave to master
S: Start condition. Sr: Repeated Start (Start without preceding stop.)

Slave Address:

write address = 0xdc = 11011100b
read address = 0xdd = 11011101b
R/W: Read/Write selection. High = read, LOW = write.
A: Acknowledge bit. NA: No Acknowledge.
Data: 8-bit data P: Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 The Two-wire Serial Interface Timing

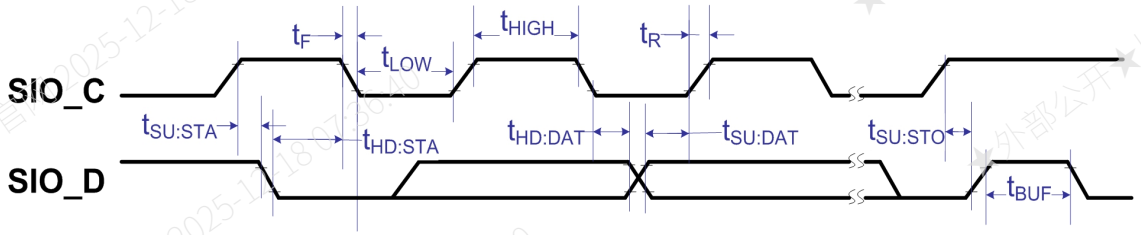


Figure 6. Two-Wire Serial Interface Timing

Table 6. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

7.4 Register Summary (full list)

Table 7. BF20A6 all registers

Address	*Name*	Width	Default value	Description
00h	*MODE_CNTL*	8	23h	Bit[7]: BYPASS_BC 1'b1:Bypass digital black cntl. 1'b0:Don't bypass digital black cntl. Bit[6]: Reserved. Bit[5:4]: Dark row select. Bit[3]: Black level adjust mode. Bit[2]: Channel select. Bit[1]: Adjust mode. Bit[0]: Adjust mode.
01h	*BLUE_GAIN*	6	1ah	Blue gain 7bit for outdoor scene, 6 bits for indoor scene.
02h	*RED_GAIN*	6	1ah	Red gain 7bit for outdoor scene, 6 bits for indoor scene.
03h	*VBLANK_PIX[12:8]*	5	00h	Bit[7:5]: Reserved. Bit[4:0] :VBLANK_PIX[12:8].
04h	*HSYST_LOCK*	8	02h	Control the rising edged of HSYNC.
05h	*HSYEN_LOCK*	8	20h	Control the falling edged of HSYNC.
06h	*DARKE_AVER*	8	RO	Current black level

Address	Name	Width	Default value	Description
07h	*DARKO_AVER*	8	RO	Current black level
0bh	*COM3*	8	00h	Bit[7]: Adjust to CCIR packet code Bit[6]: Row counter after window Bit[5]: UV output value select. Bit[4]: DAT counter delay select. Bit[3:0]: Frame counter for skip.
0ch	*AVER_LOCK*	8	32h	Bit[7:4]: Lock value1 Bit[3:0]: Lock value2
0dh	*H_HSYNC_EDGE_LOCK*	8	00h	Bit[7:4]: HSYNC rising edge[11:8] Bit[3:0]: HSYNC falling edge[11:8]
0eh	*SH_Timing*	8	1fh	SH_Timing
0fh	*SH_Timing*	8	24h	SH_Timing
10h	*SH_Timing*	8	39h	SH_Timing
11h	*SH_Timing*	8	3ch	SH_Timing
12h	*COM0*	8	20h	Bit[7]:DAT_FOUR_SWAP. 1'b1:enable 1'b0:disable. Bit[6]:High byte and Low byte crossing-over of CODE: 1'b0: Low/High 1'b1: High/Low Bit[5]: Zhan xun or mtk ccir packet swap control : 1'b1:swap , 1'b0: no swap . Bit[4]: Zhan xun or mtk ccir packet select control: 1'b1:select zhan xun ccir ,1'b0:select mtk ccir Bit[3]: 1'b0: Output 8'h00 during hblank 1'b1: Output normally during hblank Bit[2]: Process RAW and bayer RAW Selection. 1'b0:bayer RAW 1'b1:process RAW Bit[1]: DOMAIN_SEL, for Only Y mode. Bit[0]: Raw RGB Selection. YCBYCR:x0. RAW:x1.
13h	*COM8*	8	05h	Bit[7] 1'b1:AE_TAR 1'b0:AE_TAR_MODIFY Bit[6]: Select INT_TIM. Bit[5]: AE adjusts rate. Bit[4]: The MSB of the minimum integral time for every step to avoid flicker for 50HZ/60HZ light. Bit[3]: GLB_GAIN0 written when AGC disable Bit[2]: AGC Enable. Bit[1]: Digital gain switch. 1'b0:OFF 1'b1:ON. Bit[0]: AEC Enable. 1'b0:OFF , 1'b1: ON.
14h	*P_PIXEL_OE*	8	RO	Reserved.

Address	Name	Width	Default value	Description
15h	COM1	8	00h	Bit[7]: VCLK reverse ,before gated latch Bit[6]: Hsync select before window 1'b0:no hsync when vsync_dat=0 1'b1:always has hsync Bit[5]: VSYNC output selection befor packet code, 1'b0:VSYNC_IMAGE. 1'b1:VSYNC_DAT Bit[4]: VCLK reverse, after gated latch Bit[3]: HSYNC output select befor code, 1'b0:HSYNC: 1'b1:HREF. Bit[2]: 1'b0:no HREF when VSYNC_DAT=0. 1'b1:always has HREF or not. Bit[1]: Negative image enable 1'b0: Normal image. 1'b1: Negative image Bit[0]: Negative enable 1'b0: Normal 1'b1: Negative pixel
16h	COM2	8	70h	Bit[7]: Hsync mode after window: Bit[6]: Posedge and negedge of VSYNC in the MTK mode : 1'b1:enable. 1'b0:disable Bit[5]: Posedge of HSYNC in the MTK mode : 1'b1:enable 1'b0:disable Bit[4]: Posedge of HREF in the MTK mode : 1'b1:enable. 1'b0:disable Bit[3:2]: YUV Select. 2'b00:YUYV. 2'b01:UYVY. 2'b10:YVYU. 2'b11:VYUY. Bit[1]: CKGATE ahead Select. Bit[0]: GATED clock Select. 1'b0: Disable. 1'b1: Enable.
17h	HSTART	8	00h	Output Format-Horizontal Frame start high 8-bit
18h	HSTOP	8	a0h	Output Format-Horizontal Frame end high 8-bit
19h	VSTART	8	00h	Output Format-Vertical Frame start high 8-Bit
1ah	VSTOP	8	78h	Output Format-Vertical Frame end high 8-Bit
1bh	VHREF	8	00h	Bit[7:6]:Output Format-Vertical Frame(row)end low 2-Bit Bit[5:4]:Output Format-Vertical Frame(row)start low 2-Bit Bit[3:2]:Output Format-Horizontal Frame end low 2-bit Bit[1:0]:Output Format-Horizontal Frame start low 2-bit
1ch	MANU	8	80h	Manual U value
1dh	MANV	8	80h	Manual V value
1eh	SH_Timing	8	07h	SH_Timing
1fh	AVER_TAR_E	8	00h	Black level target for E col.

Address	Name	Width	Default value	Description
22h	AVER_TAR_O	8	00h	Black level target for E col.
23h	GLGAINREG	7	33h	Green Gain
24h	AE_TAR1	8	48h	Y target.
25h	K_GLB_GIAN AE_LOC	8	64h	Bit[7:4]:K_GLB_GIAN,LSB of GLB_GAIN slope. Bit[3:0]:AE_LOC,INT_TIME and GLB_GAIN lock.
26h	BLUE_GAIN_LOW_OUT	6	0dh	Bit[6:0]:The threshold of blue_gain_low_out
27h	BLUE_GAIN_HIGH_OUT	6	10h	Bit[6:0]:The threshold of blue_gain_high_out
28h	RED_GAIN_LOW_OUT	6	09h	Bit[6:0]:The threshold of red_gain_low_out
29h	RED_GAIN_HIGH_OUT	6	24h	Bit[6:0]:The threshold of red_gain_high_out
2ah	SC_CNTL3	8	98h	Bit[7]: 1'b1,pixel array reset interval also reset operate ; 1'b0,pixel array reset interval do nothing ; Bit[6]: Reset interval address select. Bit[5:0]: Reserved.
2bh	VBLANK_PIX[7:0]	8	00h	Bit[7:0] :VBLANK_PIX[7:0].
2ch	AVER_E	8	RO	Read out black aver for EB/EG
2dh	AVER_O	8	RO	Read out black aver for OR/OG
30h	SH_Timing	7	4dh	SH_Timing.
31h	SH_Timing	8	03h	SH_Timing.
32h	SC_CNTL1	8	00h	Bit[7]: 1'b1, VBLANK update netx frame. 1'b0, VBLANK update netx 2 frame. Bit[6:0]: SH_Timing.
33h	SC_CNTL2	8	26h	Bit[7:5]: Reserved. Bit[4]: 1'b1, GLB_GAIN_IN no delay. 1'b0, GLB_GAIN_IN delay one frame. Bit[3:0]: Reserved.
34h	R_COEF	8	46h	lens shading gain of R
35h	G_COEF	8	46h	lens shading gain of G
36h	B_COEF	8	46h	lens shading gain of B
39h	PURE_TH	8	58h	Bit[7:4]: Pure b threshold, multiplied by 4. Bit[3:0]: Pure r threshold, multiplied by 4.
3ah	TSLB	8	00h	Bit[7:2]:Reserved. Bit[1:0]:serial mode 2'b00:DVP 2'b01:1 bit 2'b10:2 bits 2'b11:4 bits.
3bh	AWB_CB_LIM2	8	18h	Bit[7]: Reserved. Bit[6:0]:AWB criterion: B, the threshold of B-G,for region 2.
3ch	AWB_CR_LIM2	8	18h	Bit[7]: Reserved.

Address	Name	Width	Default value	Description
				Bit[6:0]:AWB criterion: R, the threshold of R-G,for region 2.
3dh	*AWB_GR_LIM2*	8	18h	Bit[7]: Reserved. Bit[6:0]:AWB criterion: B, the threshold of G-B,for region 2.
3eh	*AWB_BR_LIM2*	8	18h	Bit[7]: Reserved. Bit[6:0]:AWB criterion: R, the threshold of G-R,for region 2.
3fh	*AWB_BR_LIM2*	8	28h	Bit[7]: Reserved. Bit[6:0]:AWB criterion: BR, the threshold of |B+R-2*G|,for region 2.
40h	*k0*	8	24h	Gamma Correction Slop Coefficients
41h	*k1*	8	30h	Gamma Correction Slop Coefficients
42h	*k2*	8	24h	Gamma Correction Slop Coefficients
43h	*k3*	8	1dh	Gamma Correction Slop Coefficients
44h	*k4*	8	1ah	Gamma Correction Slop Coefficients
45h	*k5*	8	14h	Gamma Correction Slop Coefficients
46h	*k6*	8	11h	Gamma Correction Slop Coefficients
47h	*k7*	8	0eh	Gamma Correction Slop Coefficients
48h	*k8*	8	0dh	Gamma Correction Slop Coefficients
49h	*k9*	8	0ch	Gamma Correction Slop Coefficients
4ah	*SC_CNTL0D*	5	00h	Bit[7:5]: Reserved. Bit[4]: PDM_CNTL, 1'b0:POWERDOWN run free ; 1'b1: POWERDOWN Synchronous. Bit[3]: Mirror, 1'b0: Normal image, 1'b1: Mirror image. Bit[2]: Vertical Flip, 1'b0: Normal image, 1'b1: Vertically flip image. Bit[1:0]: Reserved.
4bh	*k10*	8	0bh	Gamma Correction Slop Coefficients
4ch	*k11*	8	09h	Gamma Correction Slop Coefficients
4eh	*k12*	8	09h	Gamma Correction Slop Coefficients
4fh	*k13*	8	08h	Gamma Correction Slop Coefficients
50h	*k14*	8	07h	Gamma Correction Slop Coefficients
51h	*TARGET1*	8	0dh	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[0]).
52h	*TARGET2*	8	0eh	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[1]).
53h	*TARGET3*	8	42h	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[2]).
54h	*TARGET4*	8	4ch	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[3]).
55h	*TARGET5*	8	76h	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[4]).
56h	*TARGET6*	8	21h	Bit[7:0]: Color Correction Coefficients low 8 bit (sign bits at TARGET_SIGN2[5]).

Address	Name	Width	Default value	Description
57h	TARGET1_SK	8	37h	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[0],TARGET_H[0]}).
58h	TARGET2_SK	8	1eh	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[1],TARGET_H[1]}).
59h	TARGET3_SK	8	afh	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[2],TARGET_H[2]}).
5ah	TARGET4_SK	8	c5h	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[3],TARGET_H[3]}).
5bh	TARGET5_SK	8	55h	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[4],TARGET_H[4]}).
5ch	TARGET6_SK	8	18h	Bit[7:0]: A light Color Correction Coefficients low 8 bit ({sign bits,hign 1 bit} at {TARGET_SIGN1[5],TARGET_H[5]}).
5dh	TARGET_H	6	00h	Bit[5:0]: Control the highest value bit (bit[8]) of the A light coefficients. Bit[5]:TARGET6_SK. Bit[4]:TARGET5_SK. Bit[3]:TARGET4_SK. Bit[2]:TARGET3_SK. Bit[1]:TARGET2_SK. Bit[0]:TARGET1_SK.
5eh	GLB_GAIN_TH	8	20h	Bit[7]: Glb_gain adjust switch. 1'b1: OFF,do not be affect by glb_gain. 1'b0: ON,do adjust for glb_gain. Bit[5:0]: Used as glb_gain threshold for color martrix adjust, smaller value is for larger adjust.
5fh	AWB_SPEED OUTDOOR_EN GNGAINREG	6	21h	Bit[5:4]:AWB speed. Bit[3]: Bit[7]: outdoor_en ,outdoor model control. 1'b0:off 1'b1:on Bit[2:0]:G Channel Gain (Bit[2:0] is used as Green ain[5:3]).
60h	AVER_E_I2C	8	10h	Manual black level value for E col.
61h	AVER_O_I2C	8	10h	Manual black level value for O col.
62h	SH_Timing	8	7dh	SH_Timing.
63h	SH_Timing	7	0bh	SH_Timing.
64h	SH_Timing	7	1ah	SH_Timing.
65h	SH_Timing	7	34h	SH_Timing.
66h	SH_Timing	7	40h	SH_Timing.
67h	SH_Timing	8	9ah	SH_Timing.
68h	SH_Timing	8	6bh	SH_Timing.
69h	SH_Timing	8	6fh	SH_Timing.
6ah	SH_Timing	8	71h	SH_Timing.
6bh	SH_Timing	8	6dh	SH_Timing.
6ch	SH_Timing	8	a6h	SH_Timing.
6dh	SH_Timing	8	a7h	SH_Timing.

Address	Name	Width	Default value	Description
6eh	SH_Timing	7	09h	SH_Timing.
6fh	BRIGHT_ALL	7	00h	Bit[6]:The sign for brightness adjust: 1:positive 0:negative Bit[5:0]:value of brightness.
70h	IntCtr	8	0fh	Bit[7]:STOP_Sram--sram on/off 1'b0:on 1'b1:off Bit[6]:Raw_Switch--output rawdata select Bit[4]:G_off_En -- grid correction on/off 1'b0:off 1'b1:on Bit[3]:Edge_Switch--edge enhancement on/off 1'b0:off 1'b1:on Bit[2]:Clu_Switch--cluster correction on/off 1'b0:off 1'b1:on Bit[1]:Bp_Switch--bad pixel correction on/off 1'b0:off 1'b1:on Bit[0]:Lpf_Switch--denoise on/off 1'b0:off 1'b1:on
71h	BpcCtr	8	47h	Bit[7:4]:Bp_TH1--threshold for badpixel Bit[3]: Den_Out_En--denoise outdoor on/off 1'b0:on 1'b1:off Bit[2]: Denoise_sel--edge mean for denoise(on/off) 1'b0:select center pixel for denoise 1'b1:select edge mean for denoise Bit[1:0]:The gain value for cluster correction
72h	DenCtr1	8	27h	Bit[7:4]:Base_VAR Bit[3:0]:Base_gl_gain
73h	DenCtr2	8	68h	Bit[7:4]:Threshold to judge Bit[3:0]:Int_tim_t
74h	DenCtr3	8	a2h	Bit[7:4]:The flat region threshold value(*2) Bit[3]: Cen_Mean_sel Bit[1:0]:Edg_En_Max
75h	DenCtr4	8	89h	Bit[7:4]:Y_Th--Y_AVER threshold Bit[3:2]:Int_tim_cho Bit[0]: De_Low_En
76h	DenCtr5	8	8ah	Bit[4]: Den_Y_Aver_En Bit[3:0]: Den_Y_Aver_Th
77h	EgeCtr1	8	2fh	Bit[7:4]: Edge_TH--threshold for edge detection(*2) Bit[3:0]: Flat_TH--threshold for flat field(*2)
78h	EgeCtr2	8	23h	Bit[7:4]:Edge_Gain_P Bit[3:0]:Edge_Gain_N
79h	EgeCtr3	8	80h	Bit[7:5]: Skin denoise strength. Bit[4]: Gray_judge Bit[3]: Edg_Off_Step Bit[2]: Edg_Off_Mode Bit[1:0]:Sobel_Min

Address	Name	Width	Default value	Description
7ah	*EgeCtr4*	8	82h	Bit[7]: Sobel_en--thin edge function on/off 1'b0:off 1'b1:on Bit[4]: Low_Sh_Sw Bit[3:0]:Edg_Off_base
7bh	*SobMax*	8	ddh	{Bit[7],Bit[3]}:Gain_Denoise Bit[6:4]:Threshold for sobel difference(2^Bit[6:4]) Bit[2:0]:Threshold for sobel difference(2^Bit[2:0])
7ch	*COM_SEL1*	8	97h	Bit[7:4]:Y_DE_TH Bit[3:0]:G_OFF_TH
7dh	*TARGET_SIGN1*	6	36h	Bit[5:0]: A light Color Correction Coefficients. Bit[5]: TARGET_SEL6. Bit[4]: TARGET_SEL5. Bit[3]: TARGET_SEL4. Bit[2]: TARGET_SEL3. Bit[1]: TARGET_SEL2. Bit[0]: TARGET_SEL1.
7eh	*TARGET_SIGN2*	6	16h	Bit[5:0]: Normal light Color Correction Coefficients. Bit[5]: TARGET_SEL6. Bit[4]: TARGET_SEL5. Bit[3]: TARGET_SEL4. Bit[2]: TARGET_SEL3. Bit[1]: TARGET_SEL2. Bit[0]: TARGET_SEL1.
80h	*AE_SPEED*	8	00h	Bit[7:4] : The speed of adjusting from light to dark Bit[3:0] : The speed of adjusting from dark to light
81h	*GLB_MIN1D*	8	1bh	GLB_MIN1 8 Bits
82h	*GLB_MAX1D*	8	37h	GLB_MAX1 8 Bits
83h	*GLB_MIN2D*	8	39h	GLB_MIN2 8 Bits(test)
84h	*GLB_MAX2D*	8	5dh	GLB_MAX2 8 Bits
85h	*GLB_MIN3D*	8	39h	GLB_MIN3 8 Bits
86h	*GLB_MAX3D*	8	30h	GLB_MAX3 8 Bits
87h	*GLB_GAIN0*	7	10h	GLB_GAIN0 register.
88h	*Y_AVER*	8	RO	The Y_aver of the current frame
89h	*INT_MID_I2C*	8	45h	Bit[7:4]: The lock threshold Bit[3:0]: INT_MID
8ah	*INT_STEP_50*	8	66h	The low 8 Bits of the minimum integral time for every step to avoid flicker for 50HZ/60HZ light.
8bh	*INT_STEP*	8	03h	Steps of INT_TIM
8ch	*INT_TIM[12:8]*	5	RO	Real integration time MSB.
8dh	*INT_TIM[7:0]*	8	RO	Real integration time LSB.
8fh	*INT_MIN*	8	82h	INT_MIN select.
90h	*GAIN_BEG_4D*	8	d7h	Curve line :the fifth beginning point
91h	*GAIN_END_4D*	8	30h	Curve line :the fifth ending point

Address	Name	Width	Default value	Description
92h	GLB_HIGH	7	88h	Bit[6:4]:The threshold of gain. Bit[3]: The ending point of line 4,the msb. Bit[2]: The starting point of line 4,the msb. Bit[1]: The ending point of line 3,the msb. Bit[0]: The starting point of line 3,the msb.
94h	TAR_BASE0	8	62h	Bit[7:4]:(192+Bit[7 :4]*4) as threshold to judje one pixel whether to be over exposure pixel. Bit[3:0]:Control the start of AE.
95h	TAR_BASE1	8	88h	Bit[7:4]: is used to modify the difference of Y_AVER and modified AE_TAR) .the smaller TAR_BASE1[7:4] is ,the slower the AE adjusting. Bit[3:0]:The smallest value the target brightness can achieve.(AE_TAR*TAR_BASE1[3:0]/16).the smaller TAR_BASE1[3:0] is,the quicker the AE adjusting.
99h	DIG_GAIN_I2C	8	10h	The value of DIG_GAIN.
9ah	INT_TIM_TH	8	18h	Threshold for INT_TIME to judge outdoor scene.
9dh	Gain_OR_Last	8	RO	The value of gain_or_last[8:1] to get the GLB_GAIN0 through some operation
9eh	YBRIGHT_TH	8	b6h	Bit[7:4] : AE adjusting. Bit[3:0]: Limit the speed of AE
9fh	AE_MODE DIG_GAIN_MAX	8	14h	Bit[7]: Reserved. Bit[6]: Control the adjustive speed of digital gain 1'b0 :Y_DIFF_D[6:1] (1 time) 1'b1 :Y_DIFF_D (2 times) Bit[5]: Setps enable. Bit[4]: AE is adjusted by men, Bit[3:0]: DIG_GAIN_MAX
a0h	AWB_CTR_SET	8	09h	Bit[7]: UPDATE_MODE Bit[6]: J_CTRL6,sign white pixel selection Bit[5]: J_CTRL5, Bit[4]: J_CTRL4,combination1 selection. Bit[3]: J_CTRL3 Bit[2]: J_CTRL2,PIXEL_WP_EN setting. Bit[1]: J_CTRL1,combination2 selection. Bit[0]: AWB_ENABLE: 1'b1:AWB on 1'b0:AWB off
a1h	AWB_TH1_SET	8	10h	Bit[7:4]:AWB_LOCK, Auto white balance lock boundary. Bit[3:2]:SKIN_BGAIN_TH_L. Bit[1:0]:SKIN_RGAIN_TH_L.
a2h	BLU_GAIN_TH1	6	0bh	Bit[7:6]: Reserved. Bit[5:0]: Minimum blue gain.
a3h	BLU_GAIN_TH2	6	30h	Bit[7:6]: Reserved. Bit[5:0]: Maximum blue gain.
a4h	RED_GAIN_TH1	6	09h	Bit[7:6]: Reserved. Bit[5:0]: Minimum red gain.

Address	Name	Width	Default value	Description
a5h	RED_GAIN_TH2	6	30h	Bit[7:6]: Reserved. Bit[5:0]: Maximum red gain.
a6h	COUNT_EN	8	56h	Bit[7:4]: Region 3 counter threshold. Bit[3:0]: White pixel counter threshold.
a7h	BASE_B_GAIN	6	12h	Bit[7:6]:Reserved. Bit[5:0]:Base B gain.
a8h	BASE_R_GAIN	6	12h	Bit[7:6]:Reserved. Bit[5:0]:Base R gain.
a9h	AWB_GB_LIM	8	12h	Bit[7:6]: Reserved. Bit[5:0]:AWB criterion: B
aah	AWB_GR_LIM	8	12h	Bit[7:6]: Reserved. Bit[5:0]:AWB criterion: R
abh	AWB_BR_LIM	8	18h	AWB criterion: BR,for region 1.
ach	AWB_Y_TH	8	a8h	AWB criterion
adh	AWB_G_LIM	8	12h	The threshold for region 3.
aeh	F_GAIN_TH_H	8	59h	Bit[7:4]: B limit to estimate F light. Bit[3:0]: R limit to estimate F light.
afh	DIG_SLOPE	8	0ah	Bit[7:4]: Color Gain offset Bit[3:0]: Slop of color gain for digital gain
b0h	SAT_CTRL1	8	00h	Bit[7:4]: Select the mean of the gray section Bit[5:0]: Low light ctrl.
b1h	CB_COEF_NF	8	c6h	Cb Saturation Coefficient low 8 bit for NF
b2h	CR_COEF_NF	8	cch	Cr Saturation Coefficient low 8 bit for NF
b3h	CB_COEF_F	8	d6h	Cb Saturation Coefficient low 8 bit for F
b4h	CR_COEF_F	8	dch	Cr Saturation Coefficient low 8 bit for F
b5h	SAT_GAIN_TH	5	0ch	Bit[4:0]:The threshold of GLB_GAIN.
b6h	TEST_MODE	8	00h	Bit[7:0]: 8'h00: Normal output. Bit[7:0]: 8'h01~8'h0f : Fixed vertical bar pattern. Bit[7:0]: 8'h10~8'h1f : Fixed horizontal bar pattern. Bit[7:0]: 8'h20~8'h2f : Fixed vertical gradual pattern. Bit[7:0]: 8'h30~8'h3f : Fixed horizontal gradual pattern. Bit[7:0]: 8'h40~8'h5f : Fixed manual pattern. Bit[7:0]: 8'h60~8'h7f: Normal output.
b7h	MAN_R	8	80h	Bit[7:0]: Define R/G/B value.
b8h	GAIN_DIFF COLOR_CTRL	8	93h	Bit[7:4]: Gain_diff (Used to wipe off gain function). Bit[1]: Pure blue enable Bit[0]: Pure red enable
b9h	SKIN_GAIN_TH	8	64h	Skin select.
bah	AWB_CB_LIM1	8	12h	Bit[7:6]: Reserved. Bit[5:0]:AWB criterion: B.
bah	AWB_CR_LIM1	8	12h	Bit[7:6]: Reserved. Bit[5:0]: AWB criterion: R.
bch	SH_Timing	8	08h	SH_Timing.

Address	Name	Width	Default value	Description
bdh	SH_Timing	8	04h	SH_Timing.
beh	SH_Timing	8	07h	SH_Timing.
bfh	SH_Timing	8	09h	SH_Timing.
c0h	SH_Timing	8	0ch	SH_Timing.
c1h	SH_Timing	8	10h	SH_Timing.
c2h	SH_Timing	8	15h	SH_Timing.
c3h	SH_Timing	8	11h	SH_Timing.
c4h	SH_Timing	8	14h	SH_Timing.
c5h	SH_Timing	8	16h	SH_Timing.
c6h	SH_Timing	8	19h	SH_Timing.
c7h	SH_Timing	8	01h	SH_Timing.
c8h	SH_Timing	6	2ah	SH_Timing.
c9h	SH_Timing	6	2ch	SH_Timing.
cah	SH_Timing	8	1ah	SH_Timing.
cbh	LINE_LENGTH_OUT[7:0]	8	90h	Bit[7:0] :LINE_LENGTH[7:0].
cch	{5'B0,LINE_LENGTH_OUT[10:8]}	8	01h	Bit[7:3]: Reserved. Bit[2:0] :LINE_LENGTH[12:8].
cdh	SH_Timing	8	16h	SH_Timing.
ceh	SH_Timing	8	14h	SH_Timing.
cfh	SH_Timing	8	17h	SH_Timing.
d0h	SH_Timing	8	30h	SH_Timing.
d1h	SH_Timing	8	32h	SH_Timing.
d2h	S SH_Timing	8	7bh	SH_Timing.
d5h	CON_CTRL1	6	08h	Bit[5]: Gray section denoise switch. 1'b0:disable 1'b1:enable Bit[4]: Gray section denoise mean select. Bit[3:0]: Bright, increase brightness in low light scene.
d6h	Y_COEF	8	80h	Y Coefficient for Contrast
d8h	GAIN_BEG_0D	8	0fh	Curve line :the first beginning point
d9h	GAIN_END_0D	8	20h	Curve line :the first ending point
dah	GAIN_BEG_1D	8	21h	Curve line :the second beginning point
dbh	GAIN_END_1D	8	42h	Curve line :the second ending point
dch	GAIN_BEG_2D	8	43h	Curve line :the third beginning point
ddh	GAIN_END_2D	8	7eh	Curve line :the third ending point
deh	GAIN_BEG_3D	8	84h	Curve line :the forth beginning point
dfh	GAIN_END_3D	8	d6h	Curve line :the forth ending point
e0h	REG_PD	8	01h	Bit[7:1]: Reserved. Bit[0]: Soft PD(Analog ctrl). 1'b0: Power on. 1'b1: Power down.

Address	Name	Width	Default value	Description
e1h	*REG_DIV*	8	92h	Bit[7:5]: CLK SEL. Bit[4]: VCLK invert. 1'b0:not invert. 1'b1: invert(default). Bit[3:0]: CLK SEL
e2h	*REG_DIV2*	8	01h	Bit[7:5]: Reserved. Bit[4:3]: VCLK delay. Bit[2:0]: Reserved.
e3h	*REG_PLL*	8	82h	Bit[7]: PLL Bypass. 1'b0: Do not bypss. Fout=Fpll/ z1 1'b1: Bypass pll(default) . Fout=Fin. Bit[6]: OEN_VSYNC_CLK. 1'b0:Enable. 1'b1:Disable. Bit[5:4]: Post Div for PLL(Fout) 2'b00: Div 1(z=1)(default). 2'b01: Div 2(z=2). 2'b10: Div 4(z=4). 2'b11: Div 8(z=8). Bit[3:2]: Reserved. Bit[1:0]: PLL Pre_sel[1:0]. 2'b00: x=2. 2'b01: x=4. 2'b10: x=8(default). 2'b11: x=9. Fref=Fin/x=3MHz.
e4h	*REG_BIAS*	8	92h	Reserved.
e5h	*REG_BIAS2*	8	22h	Reserved.
e6h	*REG_COM*	8	24h	Reserved.
e7h	*REG_COM2*	8	66h	Bit[7]: OEN_HSYNC_DATA. 1'b0:Enable. 1'b1:Disable. Bit[6:0]: Reserved.
e8h	*REG_COM3*	8	a1h	Bit[7]: Reserved. Bit[6:5]: Sel for DATA drive. Bit[4]: Sel for I2C SDA drive. Bit[3:0]: LDO Sel.
eeh	*P_TH*	6	0fh	Bit[5:0]: Probability Threshold
efh	*SKIN_CTR*	3	4h	Bit[2]: 1'b0: Disable skin function, 1'b1: Enable skin function. Bit[1]: 1'b0: Disable white pixels signing function, 1'b1: Enable white pixels signing function. Bit[0]: 1'b0: display full resolution, 1'b1: only display skin area.
f0h	*INT_MAX_I2C*	6	53h	Bit[7:6]: P_OE_SEL Bit[5:0]:INT_MAX, the MAX steps of integral time

Address	Name	Width	Default value	Description
f1h	ISPBYPS	7	00h	Bit[7]:Reserved Bit[6]:Contrast enable 1'b0: enable, 1'b1: disable Bit[5]:Saturation enable 1'b0: enable, 1'b1: disable Bit[4]:CC_SP enable 1'b0: enable, 1'b1: disable Bit[3]:Color Correction enable 1'b0: enable, 1'b1: disable Bit[2]:Color Intrpolation enable 1'b0: enable, 1'b1: disable Bit[1]:GammaCorrection enable 1'b0: enable, 1'b1: disable Bit[0]:LensCorrection enable 1'b0: enable, 1'b1: disable
f2h	SCCB_RESET	1	0h	Bit[0]:SCCB_RESET 1'b0: No change 1'b1: Resets all registers to default values
f3h	BURRFILT	8	01h	Parameter for I2C start siginal filter
fbh	VER_Semiconductor	4	RO	Bit[3:0] : Product ver..
fch	PIDH_Semiconductor	8	20h,RO	Bit[7:0] : Product ID MSB.
fdh	PIDL_Semiconductor	8	a6h,RO	Bit[7:0] : Product ID LSB.

8. Package Specifications

8.1 CSP Package

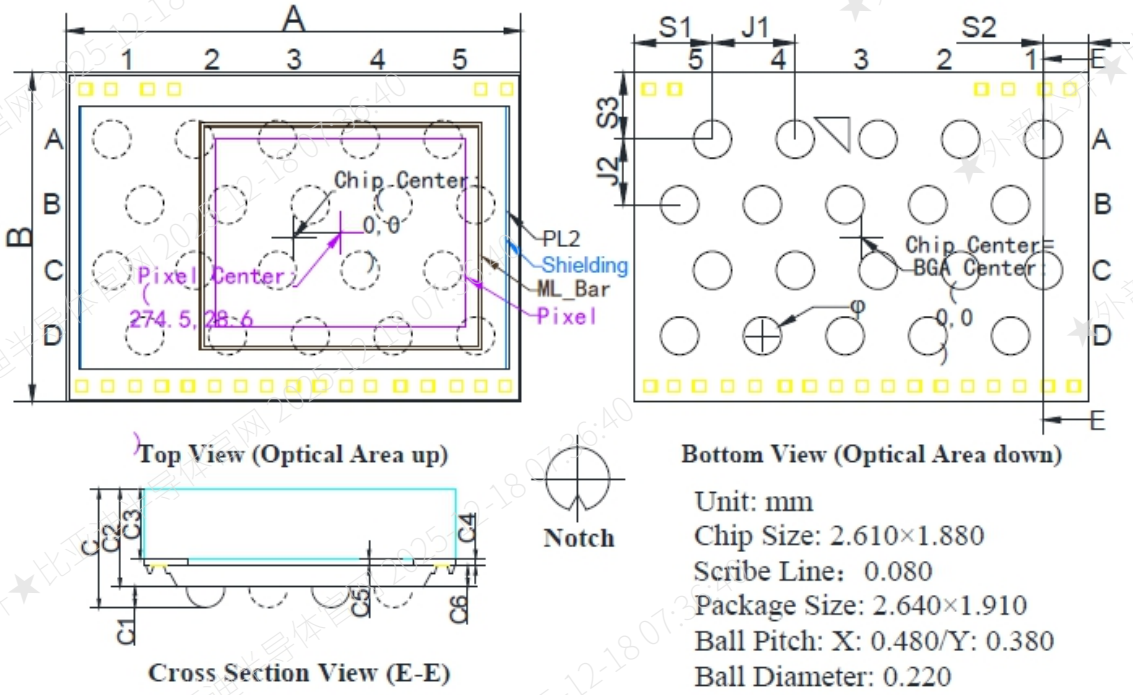


Figure 7 CSP dimension description

Table 8. CSP Dimensions

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	2.6400	2.6150	2.6650	0.103937	0.102953	0.104921
Package Body Dimension Y	B	1.9100	1.8850	1.9350	0.075197	0.074213	0.076181
Package Height	C	0.6900	0.6350	0.7450	0.027165	0.025000	0.029331
Ball Height	C1	0.1200	0.0900	0.1500	0.004724	0.003543	0.005906
Package Body Thickness	C2	0.5700	0.5400	0.6000	0.022441	0.021260	0.023622
Glass Thickness	C3	0.4000	0.3900	0.4100	0.015748	0.015354	0.016142
Cavity Wall Height	C4	0.0300	0.0260	0.0340	0.001181	0.001024	0.001339
Cavity Wall+ Epoxy Thickness	C5	0.0325	0.0275	0.0375	0.001280	0.001083	0.001476
Si Thickness	C6	0.1000	0.0950	0.1050	0.003937	0.003740	0.004134
Ball Diameter	Φ	0.2200	0.1900	0.2500	0.008661	0.007480	0.009843
Total Ball Count	N	20	/	/	20	/	/
Ball Count X Axis	N1	5	/	/	5	/	/
Ball Count Y Axis	N2	4	/	/	4	/	/
Ball Pitch X Axis 1	J1	0.4800	0.4700	0.4900	0.018898	0.018504	0.019291
Ball Pitch Y Axis 2	J2	0.3800	0.3700	0.3900	0.014961	0.014567	0.015354
Package Center to Chip Center Offset in X-Direction(Optical Area up)	ΔX	0.0000	-0.0250	0.0250	0.000000	-0.000984	0.000984
Package Center to Chip Center Offset in X-Direction(BGA Area up)	ΔY	0.0000	-0.0250	0.0250	0.000000	-0.000984	0.000984
BGA Ball Center to Chip Center Offset in X-Direction(BGA Area up)	ΔX1	0.0000	-0.0250	0.0250	0.000000	-0.000984	0.000984
BGA Ball Center to Chip Center Offset in Y-Direction(BGA Area up)	ΔY1	0.0000	-0.0250	0.0250	0.000000	-0.000984	0.000984
Package Body Edge to Ball Center Distance along X1	S1	0.4552	0.4252	0.4852	0.017921	0.016740	0.019102
Package Body Edge to Ball Center Distance along X2	S2	0.2648	0.2348	0.2948	0.010425	0.009244	0.011606
Package Body Edge to Ball Center Distance along Y	S3	0.3850	0.3550	0.4150	0.015157	0.013976	0.016339

Table 9. CSP Pin Descriptions

Pin Number	Name	Pin Type	Function/Description

Pin Number	Name	Pin Type	Function/Description
A1	VDDIO	Supply	I/O power supply:1.7~ 3.1V
A2	VCLK	Output	DVP or SPI clock output
A3	VSYNC	Output	Vertical synchronization output
A4	SCL	Input	SCCB serial interface clock input.
A5	VDD3A	Supply	Analog power 2.8V
B1	HSYNC	Output	Horizontal synchronization output
B2	D[2]	Output	DVP D[2] or SPI D[2] output
B3	D[5]	Output	DVP D[5] output
B4	XCLK	Input	System clock input.
B5	VSSA	Ground	Analog ground
C1	VSSD	Ground	Digital ground.
C2	D[1]	Output	DVP D[1] or SPI D[1] output
C3	D[4]	Output	DVP D[4] output
C4	D[7]	Output	DVP D[7] output
C5	XPD	Input	Power Down Mode Selection. 0: Normal mode. 1: Power down mode.
D1	D[0]	Output	DVP D[0] or SPI D[0] output
D2	D[3]	Output	DVP D[3] or SPI D[3] output
D3	D[6]	Output	DVP D[6] output
D4	SDA	I/O	SCCB serial interface data I/O .
D5	VDD3D	Supply	Digital power 2.8V

Note：

1. XPD : pull-down to VSSD by inner resistor.

9. Application Timing Diagram

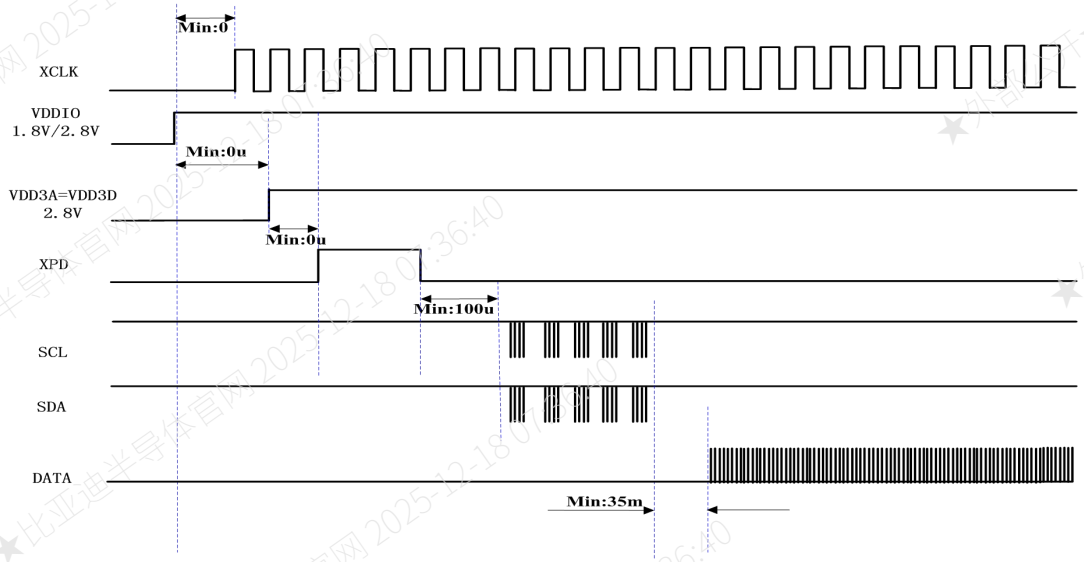


Figure 8. Power-on Sequence

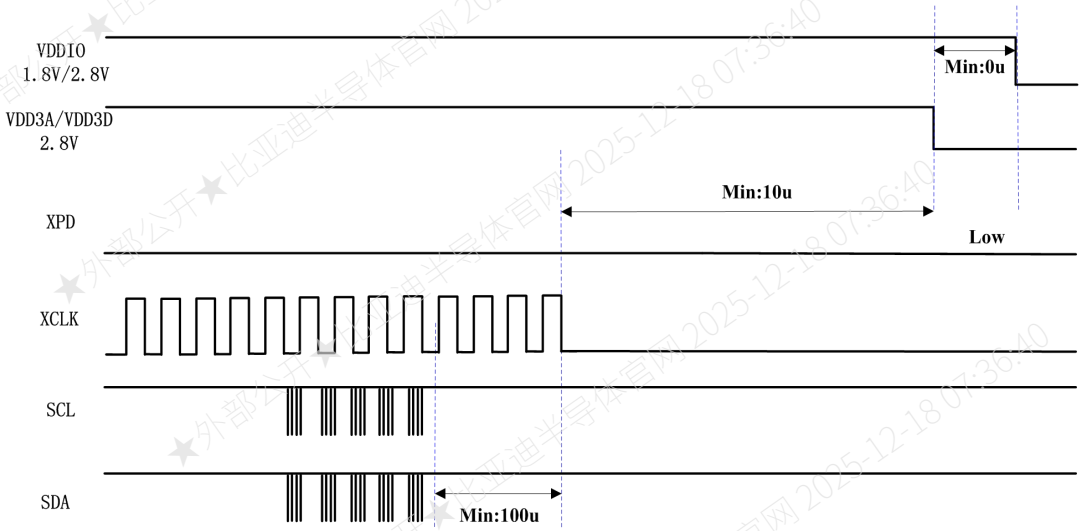


Figure 9. Power-off Sequence

RESTRICTIONS ON PRODUCT USE

- The information contained herein is subject to change without notice.
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