比亚迪半导体
Semiconductor

1/15 inch QVGA CMOS Image Sensor

BF30A2

Datasheet

Apply to：BF30A2CS

Content

1. General Description

The BF30A2 is a highly integrated QVGA camera chip which includes CMOS image sensor (CIS)，image signal processing function (ISP). It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity and very low power imaging system. The sensor consists of a 248*328 effective pixel array which has an optical format of 1/15 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, auto black level compensation and on-chip 8-bit ADC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides YCbCr 4:2:2 , RAW and only Y with SPI output interface.

This product is capable of operating at up to 15 frames per second at 24MHz master clock in QVGA resolution, with complete user control over image quality and data formatting. All required image processing functions, including exposure control, white balance control, color saturation control and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/15 inch for QVGA.
- 15 frames/sec QVGA   YUV mode @ 24MHZ input clock.
- 30 frames/sec QVGA   RAW mode @ 24MHZ input clock.
- Ultra-low dark noise at high temperature.
- Output mode: YCbCr 4:2:2,RAW,only Y
- Horizontal /Vertical mirror.
- 50/60Hz flicker cancellation.
- Auto black level control.
- Image processing function: Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation and Contrast, and Data Format Conversion.
- Package: CSP

3. Applications

- Security systems
- Cellular Phone Cameras
- PDAs
- Toys
- MP4

4. Technical Specifications

- Active pixel array: 248*328
- Pixel size: 2.5um×2.5um
- Sensitivity: 1.8 V/Lux-sec
- Dark current: 3mV/s at 40℃
- Power supply: 2.7V -3.1V for VDD3A
  1.7-3.1V for VDDIO
- Power consumption: 25mW@ QVGA output
- Standby current: 30uA
- S/N Ratio: 35 dB
- Dynamic range: 55dB
- Stable Image temperature: -10~60℃
- Optimal lens chief ray angle: 21.6º
- Package: CSP

5. Functional Overview

Figure 1. Block Diagram

BF30A2 has an active image array of 248x328 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. It has a gain control block that is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, color correction, gamma correction, data format conversion and so on.

5.1 Pixel Array

Figure 2.   Sensor Array Region

The pixel array includes 248×328 effective pixels for imaging, whose address range is from (0, 0) to (247,327). There are 6 extra dummy rows and 2 extra dark rows at the top side.

Pixel array is covered by Bayer color filters as can be seen in the figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel.

5.2 Column CDS

BF30A2 has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Lens Chief Ray Angle (CRA)

Figure 3.   CRA information

Table 1.   CRA versus image height plot

Field(%)	Image Height(mm)	CRA(degree)
0	0.00	0
0.1	0.05	2.16
0.2	0.10	4.32
0.3	0.15	6.48
0.4	0.20	8.64
0.5	0.25	10.8
0.6	0.30	12.96
0.7	0.35	15.12
0.8	0.40	17.28
0.9	0.45	19.44
1	0.50	21.6

5.4 Timing controller

- The timing controller controls the following functions
- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing

5.5 A/D converter

The analog signals are converted to digital forms one line at a time and data are streamed out column by

column. BF30A2 provides the 8-bit Raw Bayer data for ISP through an internal 8-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Gamma Correction, Bad pixel correction, Color Interpolation, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, Data Format Conversion.

6. Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Ratings
- Supply voltage (VDD3A): 2.7~ 3.1 V
- Supply voltage (VDDIO): 1.7~ 3.1 V
- Operating temperature: -30~70 ℃
- Storage temperature: -10~60℃
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2 DC Parameters

Table 2. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDD3A	Analog power supply	V	2.7	2.8	3.1	--
VDDIO	DigItal and I/O power supply	V	1.7	2.8	3.1	--
Vih	Input voltage logic "1"	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic "0"	V	--	--	0.2* VDDIO	--
Voh	Output voltage logic "1"	V	0.9* VDDIO	--	--	--
Vol	Output voltage logic "0"	V	--	--	0.1* VDDIO	--
I_vdd3a	VDD3A supply current,	mA	--	4	--	1
I_vddlo	VDDIO supply current,	mA	--	4	--	1

Note：

1. VDD3A=VDDIO=2.8V （the current in 15 fps at YUV mode and 30fps at RAW mode are nearly the same, the current in 30fps at only Y mode is max.）

6.1.3 Clock Requirement

Table 3. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	--	24	--	1
MCLK	Master clock	MHz	--	3	--	2
SCLK	two-wire serial interface clock frequency	KHz	--	400	--	3

Note:

1. XCLK is the input clock.

2. MCLK is the master clock of the system, with different output mode control, the frequency can vary.

3. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section

6.2 Electro-Optical Characteristics

Clock frequency: 24MHz.

Operating voltage: VDD3A=VDDIO=2.8V

Operating temperature: 25℃

Table 4. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	1.8	--	1
Dark current	mV/sec	--	3	--	2
S/N ratio	dB	--	35	--	--
Dynamic Range	dB	--	55	--	--
Frame Rate	fps	--	15	15	3

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.

2. Measured at dark condition for exposure time of 1s (40 Celsius).

3. With 240×320 window size at MCLK 3MHz.

6.3 Timing

6.3.1 The Sensor-core Readout Mode

Figure 4. Internal clock Timing

Figure 5.   Internal Horizontal Timing YUV4:2:2

Figure 6.   Internal Frame Timing YUV4:2:2

Figure7.   SPI Data transfer interface

Table 5.   AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_{PCLK}	$t_P = 2 \times t_{MCLK}$	--	666.6	--	ns
f_{MCLK}	Master Clock Frequency	--	3	--	MHz
f_{VCLK}	Video Clock Frequency	--	24	--	MHz
t_{LINE}	Line length	--	$294 \times t_P$	--	ns

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

Figure 8. Spectral Characteristics

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF30A2 are written and read through the two-wire serial interface. BF30A2 has two-wire serial interface slave and master. BF30A2 is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF30A2 through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to external VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of BF30A2 is 7'b1101110 (0X6e).

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A0 in the LSB of the address indicates write mode, and A1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF30A2 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

Single Write Mode Operation

S	Slave address	W	A	Register address	A	Data	A	P

Multiple Write Mode (Register address is increased automatically)[1] operation

S	Slave address	W	A	Register address	A	Data	A	· · ·

· · ·	A	Data	A	Data	A	· · ·	A	Data	A	P

Single Read Mode Operation

S	Slave address	W	A	Register address	A	· · ·

Sr	Slave address	R	A	Data	NA	P

Multiple Read Mode (Register address is increased automatically)[1] Operation

S	Slave address	W	A	Register address	A	· · ·

Sr	Slave address	R	A	Data	A	Data	A	· · ·

· · ·	A	Data	A	Data	NA	P

From master to slave   From slave to master

S: Start condition.   Sr: Repeated Start (Start without preceding stop.)

Slave Address:

write address = 0xdc = 11011100b

read address = 0xdd = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit.   NA: No Acknowledge.

Data: 8-bit data   P: Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 The Two-wire Serial Interface Timing

Figure 9. Two-Wire Serial Interface Timing

Table 6.   AC Characteristics of Two-Wire Serial Interface

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns

t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns

7.4 Register Summary (full list)

Table 7. BF30A2 all registers

Address	Name	Width	Default value	Description

00h	*SC_CNTL0D*	8	00h	Bit[7]: 1'b1:int_tim will not plus 1;
				        1'b0:int_tim will plus 1;
				Bit[6]: 1'b1:PD_RAMP signal always be 1;
				        1'b0:PD_RAMP signal will be a pluse;
				Bit[5]: 1'b0: Normal reset;
				        1'b1: Line reset 2 active lines (Double reset);
				Bit[4]: 1'b1:READEN signal always be 1;
				        1'b0:READEN signal will be a pluse;
				Bit[3]: Mirror
				        1'b0: Normal image 1'b1: Mirror image
				Bit[2]: Vertical Flip
				        1'b0: Normal image 1'b1: Vertically flip image
				Bit[1]: Windowing Control
				        1'b0: Normal output (Default value);
				        1'b1: Enable Windowing;
				Bit[0]: Reserved.

01h	*BLUE_GAIN*	6	1ah	Blue gain 7bit for outdoor scene, 6 bits for indoor scene.
02h	*RED_GAIN*	6	1ah	Red gain 7bit for outdoor scene, 6 bits for indoor scene.

03h	*SC_CNTL3*	7	44h	Bit[7]: Reserved.
				Bit[6]: 1'b1,pixel array reset interval also reset operate;
				        1'b0,pixel array reset interval do nothing ;
				Bit[5]: 1'b1: reset interval address is 335;
				        1'b0: reset interval address is 334;
				Bit[4]: 1'b1:GLB_GAIN_IN no delay;
				        1'b0:GLB_GAIN_IN delay one frame;
				Bit[3:0]:Control the delay of HSYNCE to HREF_DAT

04h	*VBLANK_PIX[7:0]*	8	00h	Dummy line low 8 Bits
05h	*TX_R[5:0]*	6	25h	Control the rising edge of TX, TX rising edge high 6 Bits

Address	Name	Width	Default value	Description
06h	*TX_F[5:0]*	6	26h	Control the falling edge of TX, TX falling edge high 6 Bits
07h	*READEN_F[7:0]*	8	7fh	Control the falling edge of READEN, READEN falling edge low 8 Bits
08h	*TX21_F1*	5	07h	Control the first falling edge of the signal (TX21)
09h	*TX22_F1*	5	0fh	Control the first falling edge of the signal (TX22)
0ah	*Col_En_R*	5	06h	Control the rising edge of Col_En .
0bh	*COM3*	8	00h	Common Control 3, Bit[7]: valid data change for adjust to ccir packet code 1'b0: normal data 1'b1: change data 0x00 to data 0x01,and change data 0xff to data 0xfe ; Bit[6]: row counter after window 1'b1: enable 1'b0: disable Bit[5]: UV output value select 1'b0: output normal value; 1'b1: output fixed value set in MANU and MANV; Bit[4]:1'b1: DAT counter delay one sclk 1'b0: no delay Bit[3:0]: skip frame counter; if FRAME_CNT_REG=0, don't skip frame; else skip as many as FRAME_CNT_REG frames;
12h	*COM0*	8	20h	Common Control 0, Bit[7]:Output Format-Vertical Frame(row)end low 1 bits. Bit[6]:output data of packet sequence ,LSB and MSB crossing-over of CODE, like Frame start packet and Data packet: 1'b0: LSB/MSB 1'b1: MSB/LSB Bit[5]: zhan xun or mtk ccir packet swap control : 1'b1:swap 1'b0: no swap . Bit[4]: zhan xun or mtk ccir packet select control: 1'b1:select zhan xun ccir 1'b0:select mtk ccir Bit[3]: 1'b0: Output 8'h00 during hblank 1'b1: Output normally during hblank bit[2:0]: 000: YUV422, 001: Bayer Raw, 011: Only Y, 101: Processed Raw.
13h	*COM8*	8	07h	Bit[7]: 1'b1: AE_TAR 1'b0: AE_TAR_MODIFY (decrease the target brightness based on the number of over exposure pixels) Bit[6]: Select INT_TIM>STEP or INT_TIM<STEP to write 1'b0: INT_TIM>STEP (steps) 1'b1: INT_TIM<STEP(rows) Bit[5]: 1'b0: AE adjusts every two frames;

Address	Name	Width	Default value	Description
				1'b1: AE adjusts every frame when in dark scene or in bright scene; Bit[4]:STEPS_EN when STEPS_EN chages,and Bit[1] is zero , AE is adjusted by men. Bit[3]: GLB_GAIN0 written is effective when AGC disable 1'b0: GLB_GAIN0 written disable; 1'b1: GLB_GAIN0 written enable; Bit[2]: AGC Enable. 1'b0:OFF(GAIN and INT_TIM can be write) ; 1'b1:ON (GAIN and INT_TIM can NOT be write); Bit[1]: 1'b1: auto AE 1'b0: manual AE step by step; Bit[0]: AEC Enable. 1'b0:OFF 1'b1: ON.
14h	*P_PIXEL_OE*	8	RO	The number of the over exposure pixels used to modify the target brightness and the adjusting speed.
15h	*COM1*	8	00h	Common Control 1, Bit[7]: VCLK reverse ,before gated latch Bit[6]: input hsync select before window 1'b0:no hsync when vsync_dat=0 1'b1:always has hsync Bit[5]: VSYNC output selection befor packet code, 1'b0:VSYNC_IMAGE 1'b1:VSYNC_DAT Bit[4]: VCLK reverse,after gated latch Bit[3]: HSYNC output select befor code, 1'b0:HSYNC 1'b1:HREF. Bit[2]: 1'b0: no HREF when VSYNC_DAT=0; 1'b1: always has HREF no matter VSYNC_DAT=0 or not; Bit[1]:Negative image enable 1'b0: Normal image 1'b1: Negative image Bit[0]:Negative enable 1'b0: Normal 1'b1: Negative pixel(if the pixel's Y>=128)
17h	*HSTART*	8	00h	Output Format-Horizontal Frame(HREF column)start high 8-bit
18h	*HSTOP*	8	f0h	Output Format-Horizontal Frame(HREF column)end high 8-bit
19h	*VSTART*	8	00h	Output Format-Vertical Frame(row)start high 8-Bit
1ah	*VSTOP*	8	a0h	Output Format-Vertical Frame(row)end high 8-Bit(low 1 bits are at COM0[7])
1ch	*Din_Set1*	6	10h	Bit[5:0]: Din_Set VALUE 1
1dh	*Din_Set2*	6	13h	Bit[5:0]: Din_Set VALUE 2
1eh	*LINE_LENGTH_LSB*	8	26h	Bit[7:0] :LINE_LENGTH[7:0].
1fh	*LINE_LENGTH_HSB*	2	01h	Bit[7:2]: Reserved. Bit[1:0] :LINE_LENGTH[9:8].
20h	*Rst_Comp_R1[5:0]*	6	1bh	Control the first rising edge of Rst_Comp
21h	*Rst_Comp_R2[5:0]*	6	1dh	Control the rising edge of Rst_Ramp

Address	Name	Width	Default value	Description
22h	Set_Ramp_R2[5:0]	6	24h	Control the third rising edge of Set_Ramp
23h	GLGAINREG	7	33h	Green Gain[2:0], Bit[6:4]: G1 Gain (Used as Green gain [2:0] of even column), Bit[2:0]: G2 Gain (Used as Green gain[2:0] of odd column).
24h	AE_TAR1	8	48h	Y target.
25h	K_GLB_GIAN AE_LOC	8	64h	Bit[7:4]:K_GLB_GIAN,LSB of GLB_GAIN slope. Bit[3:0]:AE_LOC,INT_TIME and GLB_GAIN lock.
27h	Set_Ramp_R3[6:0]	7	4eh	Control the first change point edge of Din_Set
28h	Clamp_En_F[4:0]	5	12h	Control the falling edge of Clamp_En ;
29h	Ramp_En_R1[6:0]	7	28h	Control the second rising edge of Ramp_En
2ah	Ramp_En_F1[6:0]	7	48h	Control the second falling edge of Ramp_En
2bh	Ramp_En_R2[7:0]	8	52h	Control the rising edge of Inv_En
2ch	Ramp_En_F2[7:0]	8	79h	Control the falling edge of Inv_En
2dh	Inv_En_R[7:0]	8	49h	Control the rising edge of Inverse
2eh	Tran_En_R[7:0]	8	8ch	Control the rising edge of Invcom_En
2fh	{WIN_ST,WIN_ED}	8	0fh	Bit[7:4]:When Windowing Control enable,that in window mode,X_WIN_START. Bit[3:0]:When Windowing Control enable,that in window mode,X_WIN_END.
30h	AVER_E_I2C	7	08h	Manual black level value for E col;
31h	AVER_O_I2C	7	08h	Manual black level value for O col;
32h	DARK_E_AVER[6:0]	7	RO	current frame black level calculation value for E col;
33h	DARK_O_AVER[6:0]	7	RO	current frame black level calculation value for O col;
34h	AVER_E_TAR[7:0]	7	00h	Black level target for E col;
35h	AVER_O_TAR[7:0]	7	00h	Black level target for E col;
36h	AVER_LOCK	8	32h	Bit[7:4]: lock value to update with current frame black level ; Bit[3:0]: lock value to update with previous frame black level +1 / -1;

37h	MODE_CNTL	8	13h	Bit[7]: BYPASS_BC
				        1'b1:bypass digital black cntl;
				        1'b0:don't bypass digital black cntl;
				Bit[6]:Test pattern
				         1'b1:Testpattern function on;
				         1'b0:Testpattern function off;
				Bit[5]: Test pattern mode control
				Bit[4]: dark row select
				        1'b0: select 1 dark row;
				        1'b1:select 2 dark row;
				Bit[3]:black level adjust mode
				        1'b1, use this frame black level as AVER ;
				        1'b0, use last frame black level variety 1 as AVER .
				Bit[2]:channel exchange mode
				        1'b1, on; 1'b0,off.

Address	Name	Width	Default value	Description
				Bit[1]:even channel adjust mode 1'b1, auto; 1'b0,manual. Bit[0]: odd channel adjust mode 1'b1, auto; 1'b0,manual.
38h	AVER_E	7	RO	Read out black aver for EB/EG, this value is only adjusted by analog adjustment
39h	AVER_O	7	RO	Read out black aver for OR/OG, this value is only adjusted by analog adjustment
3ah	MAN_P	8	80h	Test pattern value
40h	k0	6	24h	Gamma Correction Slop Coefficients
41h	k1	6	30h	Gamma Correction Slop Coefficients
42h	k2	6	24h	Gamma Correction Slop Coefficients
43h	k3	6	1dh	Gamma Correction Slop Coefficients
44h	k4	6	1ah	Gamma Correction Slop Coefficients
45h	k5	5	14h	Gamma Correction Slop Coefficients
46h	k6	5	11h	Gamma Correction Slop Coefficients
47h	k7	5	0eh	Gamma Correction Slop Coefficients
48h	k8	5	0dh	Gamma Correction Slop Coefficients
49h	k9	5	0ch	Gamma Correction Slop Coefficients
4bh	k10	4	0bh	Gamma Correction Slop Coefficients
4ch	k11	4	09h	Gamma Correction Slop Coefficients
4eh	k12	4	09h	Gamma Correction Slop Coefficients
4fh	k13	4	08h	Gamma Correction Slop Coefficients
51h	TARGET1	6	01h	Color Correction Coefficients 1
52h	TARGET2	6	21h	Color Correction Coefficients 2
53h	TARGET3	6	26h	Color Correction Coefficients 3
54h	TARGET4	6	05h	Color Correction Coefficients 4
55h	CON_CTRL1	6	08h	Bit[5]:Gray section denoise switch. 1'b0:disable 1'b1:enable Bit[4]: Gray section denoise mean select. Bit[3:0]:BRIGHT, increase brightness in low light scene.
56h	Y_COEF	8	80h	Y Coefficient for Contrast
57h	TARGET5	6	28h	Color Correction Coefficients 5
58h	TARGET6	6	02h	Color Correction Coefficients 6
59h	GLB_GAIN_TH	6	20h	Bit[7]: CC denoise adjust enable 0:enable 1: disable Bit[6:0] : GLB_GAIN_TH for CC adjust, GLB_GAIN>GLB_GAIN_TH, do adjust
5ah	BRIGHT_ALL	7	00h	Bit[6]: the sign for brightness adjust: 1'b1:positive 1'b0:negative Bit[5:0]:brightness value size.
67h	MANU	8	80h	Manual U value
68h	MANV	8	80h	Manual V value

Address	Name	Width	Default value	Description
6bh	*COM2*	8	70h	Common Control 2, Bit[7]: hsync mode after window: 1'b0:no hsync when vsync_dat=0; 1'b1:always has hsync no matter vsync_dat=0 or not Bit[6]:posedge and negedge of VSYNC in the MTK mode : 1'b1:enable 1'b0:disable Bit[5]:posedge of HSYNC in the MTK mode : 1'b1:enable 1'b0:disable Bit[4]:posedge of HREF in the MTK mode : 1'b1:enable 1'b0:disable Bit[3:2]: YUV_ODR 2'b00:YUYV 2'b01:UYVY 2'b10:YVYU 2'b11:VYUY Bit[1]: 1'b0: no ahead 1'b1: CKGATE ahead 0.5 SCLK Bit[0]: 1'b0: continuous clock 1'b1: GATED clock.
70h	*IntCtr*	8	0fh	Bit[7]:STOP_Sram--sram on/off 1'b0:on 1'b1:off Bit[6]:raw_Switch--output rawdata select 1'b0:output rawdata is dealed with badpixel correction and denoise 1'b1:output rawdata is input rawdata Bit[5]:skin_denoise -- skin strong denoise on/off 1'b0:on 1'b1:off Bit[4]:G_off_En -- grid correction on/off 1'b0:off 1'b1:on Bit[3]:Edge_Switch--edge enhancement on/off 1'b0:off 1'b1:on Bit[2]:Clu_Switch--cluster correction on/off 1'b0:off 1'b1:on Bit[1]:Bp_Switch--bad pixel correction on/off 1'b0:off 1'b1:on Bit[0]:Lpf_Switch--denoise on/off 1'b0:off 1'b1:on
71h	*BpcCtr*	8	47h	Bit[7:4]:Bp_TH1--threshold for bad pixel Bit[3]:Den_Out_En--denoise outdoor on/off 1'b0:on 1'b1:off Bit[2]:Denoise_sel--edge mean for denoise(on/off) 1'b0:select center pixel for denoise 1'b1:select edge mean for denoise(no bad pixel)

Address	Name	Width	Default value	Description
				Bit[1:0]:the gain value for cluster correction 2'b00:1/4 2'b01:3/8 2'b10:1/2 2'b11:3/4

72h	*DenCtr1*	8	48h	Bit[7]:reserved;
				Bit[6]:DE_DARK_SEL;
				    1'b0:low light strong denoise range from alggain 0x30 t0 0x3f
				    1'b0:low light strong denoise range from alggain 0x30 t0 0x4f
				Bit[5:0]:Base_VAR–base threshold for denoise

73h	*DenCtr2*	8	68h	Bit[7:4]:threshold to judge whether it is bad region(*2) Bit[3:0]:Int_tim_th– for outdoor denoise (*16)

74h	*DenCtr3*	8	a2h	Bit[7:4]:the flat region threshold value(*2)
				Bit[3]:Cen_Mean_sel–data select for denoise
				    1'b0:select mean value to calculate variance(flat region)
				    1'b1:select center pixel to calculate variance
				Bit[2]:DE_N_SEL– Selected old De-noise or new De-noise,
				    0: Select old De-noise
				    1: Select new De-noise
				Bit[1:0]:Edg_En_Max–maximum value add or minus on edge
				    2'b00:1/4*Y_CEN 2'b01:1/2*Y_CEN
				    2'b10:3/4*Y_CEN 2'b11:Y_CEN

75h	*EgeCtr1*	8	bfh	Bit[7:6]:OUT_DE_S–outdoor weak denoise, the denoise become weaker when this value become smaller; Bit[5:3]:Edge_TH–threshold for edge detection(*2) Bit[2:0]:Flat_TH–threshold for flat field(*2)

76h	*EgeCtr2*	8	23h	Bit[7]:Gray_judge,1'b0:gray area judge include all region;
				              1'b1:gray area judge except edge region
				Bit[6:4]:Edge_Gain_P–positive edge enhancement gain
				    3'b000:0.5 3'b001:1.0
				    3'b010:1.5 3'b011:2.0
				    3'b100:2.5 3'b101:3.0
				    3'b110:3.5 3'b111:4.5
				    else:1.0
				Bit[2:0]:Edge_Gain_N–negative edge enhancement gain
				    3'b000:0.5 3'b001:1.0
				    3'b010:1.5 3'b011:2.0
				    3'b100:2.5 3'b101:3.0
				    3'b110:3.5 3'b111:4.5
				    else:1.0

77h	*DenCtr4*	8	ffh	Bit[7:4]:dark area strong denoise scope, the denoise becomes stronger when this value becomes larger;

Address	Name	Width	Default value	Description
				Bit[3:0]:skin area strong denoise scope, the denoise becomes stronger when this value becomes larger;
78h	G_OFF_TH	8	33h	be used to choose the area to do de_grid,when STD is smaller than this value ,do de_grid, else don't do de_grid
80h	AE_SPEED	8	00h	Bit[7:4] : the speed of adjusting from light to dark Bit[3:0] : the speed of adjusting from dark to light
81h	GLB_MIN1D	8	1bh	GLB_MIN1 8 Bits
82h	GLB_MAX1D	8	37h	GLB_MAX1 8 Bits
83h	GLB_MIN2D	8	39h	GLB_MIN2 8 Bits
84h	GLB_MAX2D	8	5dh	GLB_MAX2 8 Bits
85h	GLB_MIN3D	8	39h	GLB_MIN3 8 Bits
86h	GLB_MAX3D	8	30h	GLB_MAX3 8 Bits
87h	GLB_GAIN0	7	10h	GLB_GAIN0 register.
88h	Y_AVER	8	RO	the Y_aver of the current frame
89h	INT_MID_I2C	8	45h	Bit[7:4]:the lock threshold*4 for when the next frame's P_PIXEL_OE is larger than the former frame's P_PIXEL_OE ,then update the P_PIXEL_OE value Bit[3:0]:INT_MID: the integral time when the GLB_MIN begin to become larger in order to adjust the picture more fast.
8ah	INT_STEP_50	8	66h	the low 8 Bits of the minimum integral time for every step to avoid flicker for 50HZ light.
8bh	INT_STEP	8	03h	steps of INT_TIM,use with COM8[4]&COM8[2]. can be write when COM8[4]=0 &COM8[2]=0 .
8ch	INT_TIM[15:8]	4	RO	real integration time MSB.
8dh	INT_TIM[7:0]	8	RO	real integration time LSB.
8fh	INT_MIN	8	82h	Bit[7]: 1'b0: INT_MIN is as big as the integral time of one step ; 1'b1: INT_MIN is Bit[6:0].(the minimum integral time will be INT_MIN[6:0].
90h	GAIN_BEG_4D	8	d7h	Curve line :the fifth beginning point
91h	GAIN_END_4D	8	30h	Curve line :the fifth ending point
92h	GLB_HIGH	7	88h	Bit[7:4]:the threshold of gain : TH3: GLB_HIGH[4],GLB_MIND2; TH4: GLB_HIGH[5],GLB_MIND3; TH5: GLB_HIGH[6],GLB_MAXD2. TH6: GLB_HIGH[7],GLB_MAXD3. Bit[3]:the ending point of line 4,the msb Bit[2]:the starting point of line 4,the msb Bit[1]:the ending point of line 3,the msb Bit[0]: the starting point of line 3,the msb
94h	TAR_BASE0	8	82h	Bit[7:4]:(192+Bit[7 :4]*4) as threshold to judje one pixel whether to be over exposure pixel; Bit[3:0]:control the start of AE

Address	Name	Width	Default value	Description
95h	TAR_BASE1	8	8dh	Bit[7:4]: is used to modify the difference of Y_AVER and modified AE_TAR) .the smaller TAR_BASE1[7:4] is ,the slower the AE adjusting. Bit[3:0]:the smallest value the target brightness can achieve. (AE_TAR*TAR_BASE1[3:0]/16). the smaller TAR_BASE1[3:0] is, the quicker the AE adjusting.
9ah	INT_TIM_TH	8	18h	Threshold for INT_TIME to judge outdoor scene
9dh	Gain_OR_Last	8	RO	The value of gain_or_last[9:1] to get the GLB_GAIN0 through some operation
9eh	YBRIGHT_TH	8	b6h	Bit[7:4] : the speed of AE to adjust from dark to bright.the bigger it is ,the quicker the AE adjusting. Bit[3:0]: it is set to limit the speed of AE to avoid over adjusting.the bigger it is , the quicker the AE adjusting.
a0h	UPDATE_MODE	8	87h	Bit[7:4]:AWB criterion: Y_LOW*4. Bit3]:SKIN_M_EN if the pixel adjust to white pixel conditions and skin pixel conditions at the same time: 1b0:judge white pixel first 1b1:judge skin pixel first Bit[2]:YCBCR limit enable for white pixel judgement,(Y-CB-CR)>YCBCR_LIMIT(0xae); Bit[1]:UPDATE_MODE 0:RGAIN/BGAIN can be write if AWB_EN=0 strides over vsync's negedge,else can not be writen 1:RGAIN/BGAIN can be write no matter AWB_EN=0 strides over vsync's negedge or not Bit[0]:AWB_ENABLE: 1:AWB on 0:AWB off
a1h	AWB_TH1_SET	8	93h	Bit[7]:OUTDOOR_EN, outdoor enable. Bit[6:4]:G Channel Gain (Bit[2:0] is used as Green Gain[5:3]). Bit[3:0]:AWB_LOCK, Auto white balance lock boundary;
a2h	BLU_GAIN_TH1	6	0ah	Bit[7:6]: Reserved; Bit[5:0]: Minimum blue gain for indoor scene.
a3h	BLU_GAIN_TH2	6	30h	Bit[7:6]: Reserved; Bit[5:0]: Maximum blue gain for indoor scene.
a4h	RED_GAIN_TH1	6	08h	Bit[7:6]: Reserved; Bit[5:0]: Minimum red gain for indoor scene.
a5h	RED_GAIN_TH2	6	30h	Bit[7:6]: Reserved; Bit[5:0]: Maximum red gain for indoor scene.
a7h	CB_TARGET	8	80h	Cb frame average target value
a8h	CR_TARGET	8	80h	Cr frame average target value
a9h	CB_LIMIT	7	1eh	Bit[7:6]: Reserved; Bit[5:0]:AWB criterion: CB, the threshold of |CB-CB_TARGET*4|.
aah	CR_LIMIT	7	19h	Bit[7:6]: Reserved;

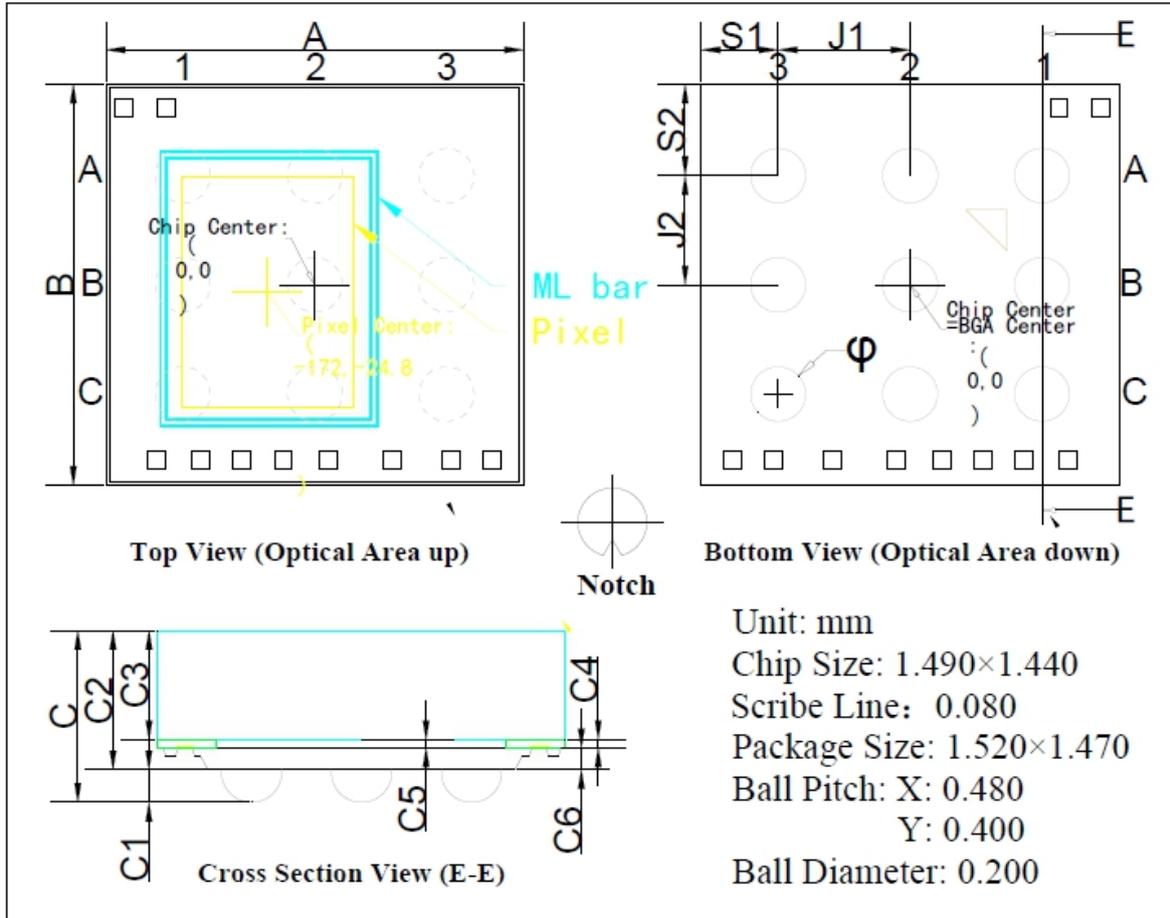| Address	Name	Width	Default value	Description
				Bit[5:0]:AWB criterion: CR, the threshold of |CR-CR_TARGET*4|.
abh	*CBCR_LIMIT*	8	1eh	Bit[7:0]:AWB criterion: |CR-CR_TARGET|+|CB-CB_TARGET*4|.
aeh	*YCBCR_LIMIT*	8	40h	AWB criterion :Y-(CB+CR)>YCBCR_LIMIT
afh	*DIG_SLOPE*	8	0ah	Bit7:4]: Color Gain offset,the practice of gain = color gain - gain_offset*2 Bit[3:0]:slop of color gain for digital gain
b1h	*CB_COEF_NF*	8	c6h	Cb Saturation Coefficient low 8 bit for NF
b2h	*CR_COEF_NF*	8	cch	Cr Saturation Coefficient low 8 bit for NF

b3h	*SAT_CTRL1*	8	00h	Bit[7:4]:used to select the mean of the gray section for test,GRAY_TH*2.
				
				Bit[3]:the switch of low light saturation.
				
				Bit[2]:the switch of low light scene decrease saturation(use with 0xb4).
				
				Bit[1:0]:low light saturation
				
				      2'b00:decrease saturation if Y < 8.
				
				      2'b01:decrease saturation if Y < 16.
				
				      2'b1x:decrease saturation if Y < 32.

b4h	*SAT_GAIN_TH*	5	0ch	Bit[4:0]:the threshold of GLB_GAIN for low light scene decrease saturation.
c8h	*BLUE_GAIN_LOW_OUT*	7	13h	Bit[6:0]:The threshold of blue_gain_low_out
c9h	*BLUE_GAIN_HIGH_OUT*	7	16h	Bit[6:0]:The threshold of blue_gain_high_out

cah	*VREG*	8	03h	Bit[7]: VCLK delay1 select
				
				  1'b0: delay 0ns(default);
				
				  1'b1: delay 6ns;
				
				Bit[6]: SCLK delay select
				
				  1'b0: delay 0ns(default);
				
				  1'b1: delay 3ns;
				
				Bit[5:4]: VCLK delay2 select
				
				  2'b00: delay 0ns(default);
				
				  2'b01: delay 3ns;
				
				  2'b10: delay 6ns;
				
				  2'b11: delay 9ns;
				
				Bit[3:2]:Signal-chain clock frequency select
				
				  2'b0x: 2x PCLK
				
				  2'b10: 1/2 system clock;
				
				  2'b11: system clock;
				
				Bit[1]: counter clock select
				
				  1'b0: normal;
				
				  1'b1: reverse;
				
				Bit[0]: system clock frequency select
				
				  1'b0: 1/2 input clock;
				
				  1'b1: input clock;

cbh	*REG_COM*	8	66h	Bit[7:4]:i-bias for com2: 4'b0000:i=10uA 0001~1111:i=0.5uA*Bit[7:4]

Address	Name	Width	Default value	Description
				Bit[3:0]:i-bias for com1: i=0.5uA*Bit[7:4]

cch	*REG_COM2*	8	52h	Bit[7:6]:LDO output control :
				
				    2'b00:1.70V 2'b01:1.80V 2'b11:1.90V 2'b11:2.00V
				
				Bit[5:3]: control bias of pixel:
				
				  3'b000:1uA 3'b001:1.5uA 3'b010:2uA 3'b011:3uA
				
				  3'b100:4uA 3'b101:5uA 3'b110:6uA 3'b111:7uA
				
				Bit[2:0]: VDDC voltage select:
				
				  v=0.8V+Bit[2:0]

cdh	*REG_COM3*	8	4ch	Bit[7]:input clock diglitch enable
				
				    1'b0:disable 1'b1:enable
				
				Bit[6]:reserved
				
				Bit[5]:LDO mode
				
				    1'b0:LDO work enable 1'b1:LDO work disalbe
				
				Bit[4:2]:reserved
				
				Bit[1]:clk_dec_sel
				
				  1'b0: decoder delay 2ns;
				
				  1'b1: decoder delay 5ns;
				
				Bit[0]: ramp clock frequency select
				
				  1'b0: 1/2 clock 1'b1:normal clock

ceh	*REG_BIAS*	8	b2h	Bit[7:5]: VDDP output select:
				
				    v=2.0V+Bit[7:5]
				
				Bit[4:0]: control the bias current of ramp:
				
				    i=3.1uA+0.08uA*Bit[4:0]

cfh	*PDA_REG*	8	b1h	Bit[7]: SDA output drive capability control
				
				  1'b0: 4mA 1'b1: 8mA(default);
				
				Bit[6:5]: SD/VCLK output drive capability
				
				 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA
				
				Bit[4]:output SD/VCLK pad tri state:
				
				  1'b1:tri state 1'b0:normal
				
				Bit[3]: reserved
				
				Bit[2]: powerdown VDDP control:
				
				    1'b0:VDDP normal
				
				     1'b1:Powerdown VDDP,(when powerdown VDDP,VDDP=VDD3A)
				
				Bit[1]: reserved
				
				Bit[0]: Soft sleep mode
				
				  1'b0: disable standby mode;
				
				  1'b1: enable standby mode(default);

d3h	*RED_GAIN_LOW_OUT*	7	0ch	Bit[6:0]:The threshold of red_gain_low_out

Address	Name	Width	Default value	Description
d4h	*RED_GAIN_HIGH_OUT*	7	26h	Bit[6:0]:The threshold of red_gain_high_out
d8h	*GAIN_BEG_0D*	8	0fh	Curve line :the first beginning point
d9h	*GAIN_END_0D*	8	20h	Curve line :the first ending point
dah	*GAIN_BEG_1D*	8	21h	Curve line :the second beginning point
dbh	*GAIN_END_1D*	8	42h	Curve line :the second ending point
dch	*GAIN_BEG_2D*	8	43h	Curve line :the third beginning point
ddh	*GAIN_END_2D*	8	7eh	Curve line :the third ending point
deh	*GAIN_BEG_3D*	8	84h	Curve line :the forth beginning point
dfh	*GAIN_END_3D*	8	d6h	Curve line :the forth ending point
eeh	*P_TH*	6	0fh	Bit[5:0]:Probability Threshold
efh	*SKIN_CTR*	3	4h	Bit[2]: 1'b0: Disable skin function, 1'b1: Enable skin function; Bit[1]: 1'b0: Disable white pixels signing function, 1'b1: Enable white pixels signing function; Bit[0]: 1'b0: display full resolution, 1'b1: only display skin area;
f0h	*INT_MAX_I2C*	6	d3h	Bit[7:6]: P_OE_SEL (what is P_OE_SEL) 2'b00:/2^{15} 2'b01:/2^{16} 2'b10:/2^{17} 2'b11:/2^{18} Bit[5:0]:INT_MAX, the MAX steps of integral time
f1h	*ISPBYPS*	6	0h	Bit[7:6]:reserved Bit[5]:Contrast enable 1'b0: enable, 1'b1: disable Bit[4]:CC_SP enable 1'b0: enable, 1'b1: disable Bit[3]:Color Correction enable 1'b0: enable, 1'b1: disable Bit[2]:Color Interpolation enable 1'b0: enable, 1'b1: disable Bit[1]:Gamma Correction enable 1'b0: enable, 1'b1: disable Bit[0]:saturation enable 1'b0: enable, 1'b1: disable
f2h	*SCCB_RESET*	1	0h	Bit[7:1]:reserved Bit[0]:SCCB_RESET 1'b0: No change 1'b1: Resets all registers to default values
fbh	*VER_Semiconductor*	4	fh,RO	Version
fch	*PIDH_Semiconductor*	8	3bh,RO	Product ID MSB
fdh	*PIDL_Semiconductor*	8	02h,RO	Product ID LSB

8. Package Specification

Top View (Optical Area up)

Notch

Bottom View (Optical Area down)

Cross Section View (E-E)

Unit: mm
Chip Size: 1.490×1.440
Scribe Line: 0.080
Package Size: 1.520×1.470
Ball Pitch: X: 0.480
　　　　　　Y: 0.400
Ball Diameter: 0.200

Die Center: (X:0, Y:0)

Pixel Array Center: (X:-172 um , Y:-24.8um)

Figure 10. CSP dimension description
Table 7　CSP Dimensions

	Symbol	Nominal	Min.	Max.
		Unit（μm）		
Package Body Dimension X	A	1520	1495	1545
Package Body Dimension Y	B	1470	1445	1495
Package Height	C	650	595	705
Ball Height	C1	100	70	130
Package Body Thickness	C2	550	520	580
Glass Thickness	C3	400	390	410
Cavity wall height	C4	30	26	34
Cavity wall+ Epoxy Thickness	C5	32.5	27.5	37.5

Si Thickness	**C6**	80	75	85
Ball Diameter	**Φ**	200	170	230
Total ball count	**N**	9		
Ball count X axis	**N1**	3		
Ball count Y axis	**N2**	3		
Pins pitch X axis	**J1**	480	470	490
Pins pitch Y axis	**J2**	400	390	410
Package Center to Chip Center Offset in X-Direction(Optical Area up)	**X**	0	-25	25
Package Center to Chip Center Offset in X-Direction(BGA Area up)	**Y**	0	-25	25
BGA Ball Center to Chip Center Offset in X-Direction(BGA Area up)	**X1**	0	-25	25
BGA Ball Center to Chip Center Offset in Y-Direction(BGA Area up)	**Y1**	5	-20	30
Package Body Edge to Ball Center Distance along X	**S1**	280	250	310
Package Body Edge to Ball Center Distance along Y	**S2**	335	305	365

Table 8 Ball Matrix Table

	1	2	3
A	VDD3A	VSSA	SCL
B	VDDIO	SDA	SD
C	PDN	XCLK	VCLK

Table 9 Pin Descriptions

PIN Num.	PIN Name	PIN Type	Function/Description
A1	VDD3A	PWR/GND	Analog power(2.7~3.1V)
A2	VSSA	PWR/GND	Analog and Digtal ground
A3	SCL	Input	Two-wire serial interface clock.
B1	VDDIO	PWR/GND	I/O and Digital power(1.7~3.1V)
B2	SDA	Input/Output	SCCB serial interface data I/O
B3	SD	Output	SPI output data
C1	PDN	Input	Power down mode ON/OFF selection: 0:work normal 1:Power down

C2	XCLK	Input	System clock Input
C3	VCLK	Output	SPI output clock

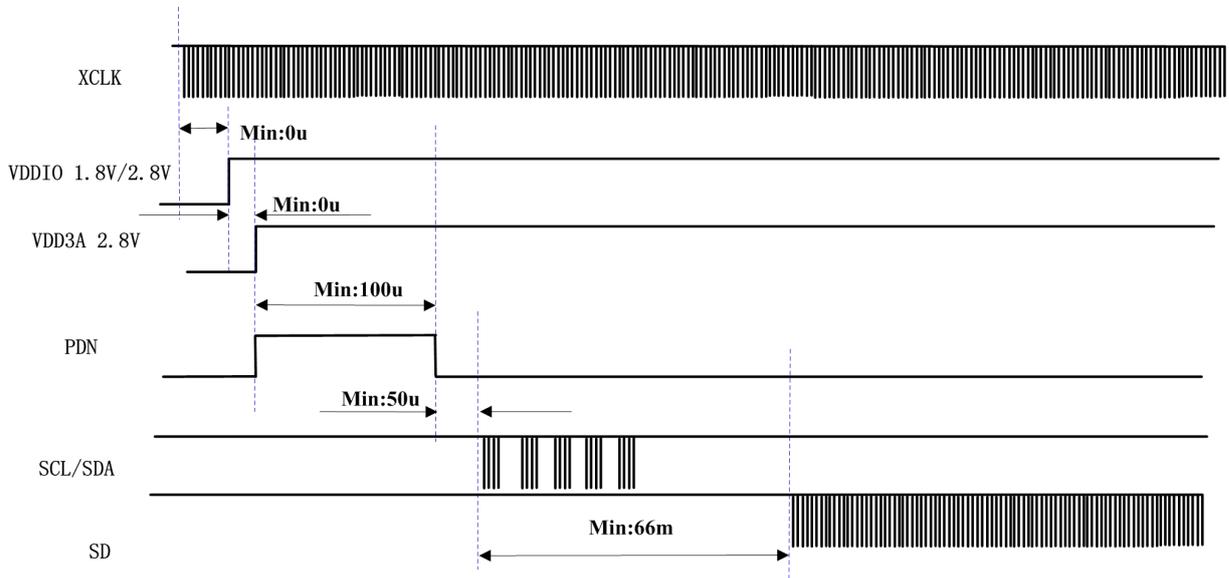# 9. Application Timing Diagram
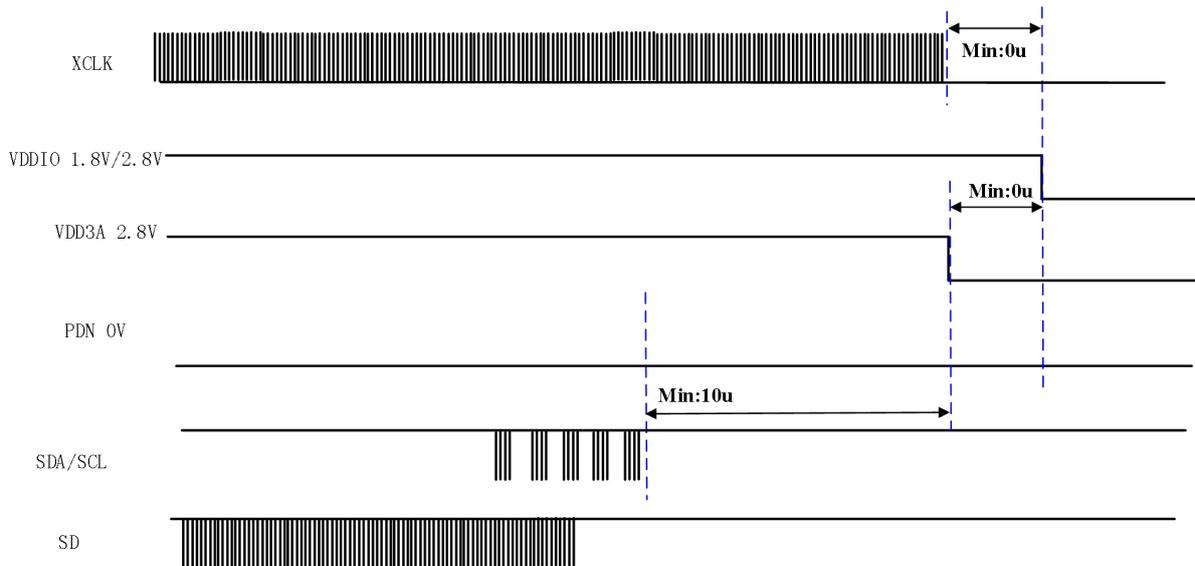

Figure 11. Power-on Sequence

Figure 12. Power-off Sequence

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